

3.5 HARDWARE JUMPERS

3.5.1 DAC/ADC Jumpers

The illustration is an abbreviated pattern of the IC-03 DAC/ADC jumpering scheme which exists on the P/C Module.

There are 256 DACs which are addressed via CSR addresses C000_0000 through C000_00FF inclusive. DAC address 00 (Hex), will always set the threshold voltage on the uppermost trace which is the threshold for the discriminator connected to the output of the summed channel which takes the sum of channel -1 and channel 0 (Σ -1,0). Likewise DAC address 01 (Hex), will always set the threshold voltage on the trace immediately below the uppermost trace which is the threshold for the discriminator connected directly to the individual channel #0 input. DAC address 02 (Hex), will always set the threshold voltage for the discriminator connected to the output of the summed channel which takes the sum of channel 0 and channel 1 (Σ 0,1). DAC address 03 (Hex), will always set the threshold voltage for the discriminator connected directly to the individual channel #1 input. This pattern continues for the 256 DACs and the 256 discriminator threshold setting inputs.

It should be obvious that if all 256 DAC's are employed, no jumpers are required and each discriminator has an individual DAC to control it's threshold. However, in the event that only 4 of the 256 DAC's are mounted on the P/C Module, the jumpers would probably be applied such that DAC 00 (hex) would drive every other sum channel. i.e., Σ (0), Σ (1,2), Σ (3,4), Σ (5,6) etc. DAC 01 (hex) would drive the even individual channels; DAC 02 (hex) would drive sum channels Σ (0,1), Σ (2,3), Σ (4,5), Σ (6,7) etc., and DAC 03 (hex) would drive the odd, individual channels.

The common choices of DAC populations are 4,8,16,32,64,128 or 256 which corresponds to 1,2,4,8,16,32 and 64 IC-03 packages. It seems reasonable to assume that for four DAC's every fourth threshold lead would be connected together and so on. However, any and all possibilities exist for connecting DAC outputs to threshold inputs and the method used may be dictated by the detector geometry.

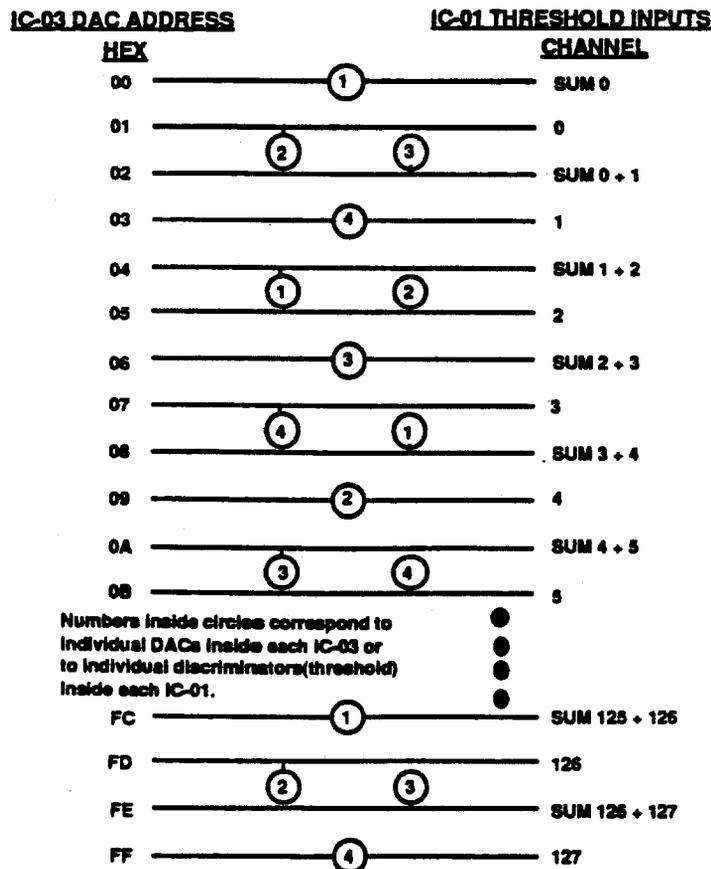


Figure 21: DAC/ADC Jumpering

3.5.2 CSR10 Jumpers

The value found in CSR10 corresponds to the configuration of three, two position jumpers(JU2, JU3, and JU4) that connect a signal trace to ground(GND) or +5V. The physical module location of the three posts for each jumper, and their connections are shown below. Table 1 on the following page provides the relationship between DAC population, jumper location, CSR10 readback and lowest ordered address for each DAC chip.

When less than 256 DAC's are utilized, the P/C module will be populated from the lowest address onward without skipping addresses, this is done by a mapping routine within the EPM5128 programmable PAL. It has been done this way to make the DACs accessible by block transfer. The PAL receives a 3 bit code from the jumpers to indicate the number of IC-03 DAC/ADC chips mounted and covers the sequential DAC address it receives from an external source to the appropriate DAC module address. I.E. if only two IC-03s(8 DACs) are used and located at DAC board address 0 through 3(U97) and DAC board address 64 through 67(U129), the PAL knowing from the jumpering scheme will only accept DAC addresses 0 through 7 from an external source and in turn converts external address 0 to DAC board address 0 and so on up to external address 7 to DAC board address 67. When less than 256 DACs are employed the IC-03s physical location is important to insure that the external address received is converted to the appropriate DAC board address. The physical locations for the common number of IC-03s used are shown in Table 2 on the following page.

CSR10 JUMPERING DIAGRAM

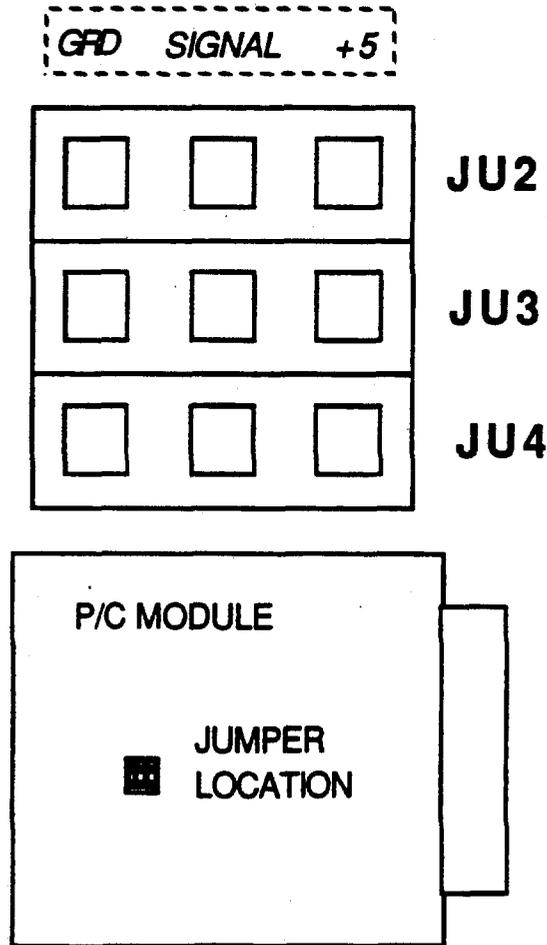


Figure 22: CSR10 Jumpering

Table 1

Jumper Numbers			# of DACs	CSR10 Value	First DAC board address of each IC-03
JU2	JU3	JU4			
Gnd	Gnd	Gnd	????	0	This is a special case, unique to the user.
Gnd	Gnd	+5V	4	1	0
Gnd	+5V	Gnd	8	2	0,80
Gnd	+5V	+5V	16	4	0,40,80,C0
+5V	Gnd	Gnd	32	8	0,20,40,60,80,A0,C0,E0
+5V	Gnd	+5 V	64	10	0,10,20,30,40,50,60,70,80,90,A0,B0,C0,D0,E0,F0
+5V	+5V	Gnd	128	20	0,8,10,18,20,28,30,38,40,48,50,58,60,68,70,78,80,88,90,98,A0,A8,B0,B8,C0,C8,D0,D8,E0,E8, F0,F8
+5V	+5V	+5V	256	40	All addresses from 00 through FF inclusive are valid

Table 2

Number of IC-03s mounted(#DACs)	IC-03 Physical location on module
1(4)	U97
2(8)	U97, U129
4(16)	U97, U113, U129, U145
8(32)	U97, U105, U113, U121, U129, U137, U145, U153
16(64)	U97, U101, U105, U109, U113, U117, U121, U125, U129, U133, U137, U141, U145, U149, U153, U157
32(128)	U97, U99, U101, U103, U105, U107, U109, U111, U113, U115, U117, U119, U121, U123, U125, U127, U129, U131, U133, U135, U137, U139, U141, U143, U145, U147, U149, U151, U153, U155, U157, U159
64(256)	ALL LOCATIONS

4.0 P/C MODULE - TESTING AND CALIBRATION

4.1 UNPOWERED TEST

A test should be performed to check for shorts between the power planes (layers) of the P/C module. The test should verify no direct connection between any of the following power planes: -5.2V, -3.5V, -2V, -.8V top, -.8V bottom, +5V, +3.5V, +1.25V, and ground. The test can be done with an OHM METER. Connection to the power plane can be found at the following locations, with the measured impedances between the power and ground plane with the PC board fully assembled (number of IC-03s equals four).

-5.2V = right side of D5	= 8 ohm
-3.5V = right side of fuse f4	= 3 ohm
-2V = right side of fuse f1	= 22 ohm
-.8V top = right side of CR2	= 23 ohm
-.8V bottom = right side of CR4	= 23 ohm
+5V = right side of fuse f6	= 400 ohm(90 ohm with EPM5128 installed)
153 = right side of fuse f2	= 580 ohm
+1.25V = case of Q1	= 73 ohm
GROUND = left side of D5	

NOTE: Right side is towards the front of the board where the LABEL is located. The drawing "POWER TEST POINT DETAILS"#2563.000-MD-215808 shows the power pin locations of various devices on the top side of the board, this should help in finding shorts.

4.2 AUTOMATED TESTING

There is an "Acceptance Test Description" document that uses two software packages to verify whether a P/C module is acceptable from an outside vendor. This document can be found in APPENDIX A.

4.3 CALIBRATION

Adjusting the value at which the **TEMP** LED on the front panel of the P/C module will turn on is the only calibration needed for the module. Adjusting trim pot R295 sets the temperature at which the LED will turn on and off, the setting of R295 controls the voltage on pin 2 of U185. If pin 3 of U185 which is connected to the LM35 temperature sensor is at a more positive value than pin 2 of U185 the LED will turn on. The voltage on pin 2 should be set to 0.5V this corresponds to 50 degrees Celsius. The LM35 will output to pin 3 of the U185 a 10 mV per degree Celsius voltage level. If the temperature rises above 50 degrees Celsius(0.5V on pin 3) the LED will turn on. The LED will turn off if the temperature falls below 50 degrees Celsius. The **TEMP** LED and associated circuitry can be tested by adjusting R295 for a voltage on pin 2 of U185 that is less than the value on pin 3 of U185, the lower voltage should cause the **TEMP** LED to turn on.

5.0 APPENDICES

- APPENDIX A - TEST SOFTWARE**
- APPENDIX B - FASTBUS INTERFACE PAL PROGRAM**
- APPENDIX C - POSTAMP/COMPARATOR MODULE - SCHEMATIC**
- APPENDIX D - MODULE DRAWINGS**
- APPENDIX E - DATA SHEETS**

APPENDIX A - TEST SOFTWARE

This appendix contains an acceptance criteria specification that pertains to the testing of the POSTAMP/COMPARATOR printed circuit board.

POSTAMP/COMPARATOR MODULE - ACCEPTANCE TEST DESCRIPTION

The party performing the acceptance test on the POSTAMP/COMPARATOR module should be familiar with the "IEEE Standard FASTBUS Modular High-Speed Data Acquisition and Control system"(ANSI/IEEE Std. 960-1986), the POSTAMP/COMPARATOR HARDWARE DESCRIPTION-HN100, and the two software packages listed below which the acceptance criteria is based upon. Questions pertaining to the documents should be addressed to the appropriate originator.

SILICON STRIP DETECTOR (SSD)

System Test Software Guide

Version: 0 15 march 1991

Originators:

Wolfgang Kowald Duke University

EXP.771 #708-840-4250

Panagiotis Spentzouris UCA

EXP.771 #708-840-4250

Dave Slimmer Fermilab

Computing Dept. #708-840-4334

SILICON STRIP DETECTOR SYSTEM "SINGLE BOARD DIAGNOSTICS TESTS"-PN434

Software Description

Version: 1 4/25/91

Originator:

Garry R. Moore Fermilab

Computing Dept. #708-840-4059

POSTAMP/COMPARATOR HARDWARE DESCRIPTION-HN100

Complete Module Documentation Manual

Version: 3 5/7/91

Originators:

Merle Haldeman Fermilab

RD/DEG group #708-840-3958

Scott Holm Fermilab

RD/DEG group #708-840-4340

Bruce Merkel Fermilab

RD/DEG group #708-840-3263

In order for the PC module to be accepted, the PC module must pass the following four tests.

1. PC TEST

Refer to the "SINGLE BOARD DIAGNOSTICS TESTS" documentation listed above.

PC_TEST is a menu driven software tool capable of effectively testing and/or exercising all FASTBUS accessible circuitry of the POSTAMP/COMPARATOR module. The test should be run in the "Exercise Postamp Comparator" mode; this is #3 under the PC_TEST main menu. This option will fully exercise all FASTBUS accessible circuitry of the PC module including all geographical address, secondary address, and DAC/ADC circuitry.

ACCEPTANCE- The software will respond with errors if the module responds incorrectly. The module is unacceptable when any errors are reported.

EXCEPTIONS: A part of the test writes and then reads a series of IC-03 DAC values, the software will respond with an error if the DAC value read back is more than plus or minus one LSB different than the written value. The module however, will be accepted when the DAC value read back is within two LSB's of the written value.

Refer to the "SILICON STRIP DETECTOR (SSD)" documentation listed on page 1 for the remaining three tests.

2. PC test counter test

This test uses an 8-bit counter on the PC module to generate 256 patterns used for testing the output portion(IC-02 and IC-04 ASIC's) of the PC module. The 8-bit counter cycles through 256 output pattern possibilities which are sent to the IC-02 and IC-04 test inputs; t1 and t2. The outputs of the IC-02s and IC-04s provide 256 different 128-bit patterns which are sent to the DE module through the FASTBUS auxiliary backplane. This test effectively tests the outputs of all IC-02 and IC-04 ASIC's as well as their connections to the backplane. The DE module has 256 memory locations which are continually being loaded with the 256 pattern possibilities. In this test an individual DE memory location is always being loaded with the same pattern generated by the PC module test counter.(Refer to section 5.4.2 PC test counter test and to APPENDIX A for test counter patterns).

ACCEPTANCE- The PC module is acceptable if no errors occur. The software will know in which memory location in the DE module each pattern generated by PC module's IC-02 and IC-04 ASICs are stored. When a memory location in the DE module is read by the software, the 128-bit pattern in that location is compared with the 128-bit pattern that was expected for that location. An error is reported if the values do not match.

3. PC channel characterization tests

This test characterizes individual and sum channel threshold voltage sensitivity for the PC module discriminator electronics. Characterizing a channel involves placing a test signal at a channel input and then scanning through the threshold setting DAC, value range with the software recording the highest threshold voltage(DAC value) at which the channel discriminator was able to detect the input test signal. The test should be performed in the default mode(DAC vs CHANNEL mode). In this mode, five separate routines need to be run on the module. These routines are listed in a menu that is displayed after "PC channel characterization test"(h) is selected from the System test menu. Invoking any one of the routines, automatically sets up the PC module for that

routine, i.e. turning on individual channel or sum channel mode, and placing the PC module in the RUN mode.

The first routine, "INDIVIDUAL CHANNEL", tests all individual channels of the PC module. The software performs in the following way: the TSM module's 256 word by 128 bit memory (refer to TSM document#) is loaded with a pattern of alternating words consisting of all A's and 5's, which means adjacent bits in a given word have opposite values as well as a given bit in adjacent memory addresses. The TSM module feeds this pattern to the LS module (refer to LS module documentation#) which continually places this pattern at the PC module input. The DE continuously updates its 256 memory locations with the 128-bit pattern that the PC module outputs through the FASTBUS auxiliary backplane. At the start, all DACs are set to the highest value in their range (1.25v) and at some instance the software performs 8 nonconsecutive reads of a DE memory location, recording which if any of the 128 channels were on (hit) during each of the 8 reads. The DAC value is then lowered 1 LSB (5mv) and the DE module memory is read 8 more times, this continues until the DACs are at their lowest value in their range (0mv). A graph is made that shows the DAC values at which a channel responded to 8 out of 8 reads with the channel on (hit) and also when the channel responds at least once but less than 8 out of 8 times.

The remaining four routines test the SUM channels. Each routine uses a different pattern such as 1's, 2's, 4's or 8's, i.e. for the 2's pattern every 2nd channel of a 4 channel combination will be toggling on and for the 8's pattern every 4th channel of a 4 channel combination will be toggling on. A graph is made for each routine. In the SUM channel mode when placing an input signal on one channel the adjacent channels also receive this input signal, therefore the adjacent channels should also turn on and the graphs should reflect this. (Refer to section 5.4.6 PC Channel Characterization Tests).

ACCEPTANCE- The input signal from the LS module should be set for a 40mv peak to peak differential amplitude. The PC module passes the test if the resulting graphs that are produced by the software are as follows. **(SHOW GRAPHS)** The DAC values of all channels may vary no more than plus or minus 15 counts from the norm, i.e. if the norm is at the DAC value of 90, acceptable DAC values range from 75 to 105. A module is unacceptable if a channel is characterized outside of the plus or minus 15 count range.

4. PC Crosstalk Test

PC Crosstalk test will test the ability of the PC module to reject crosstalk to other channels from an input signal of substantial amplitude on a certain other channel. The Crosstalk test uses the TSM and LS modules as in the PC characterization test. In this test the TSM memory is loaded with a 1 in one of the 128 bits of the first word and the remaining 255 words have a 0 in all 128 bits. This means that 1 channel is being stimulated with a 18.9ns pulse every 4.8us. The TSM module feeds this pattern to the LS module which continuously places the pattern at the PC module input, meanwhile the DE is continuously updating its 256 memory locations with the 128-bit pattern that the PC module outputs through the FASTBUS auxiliary backplane. Initially, all DACs are set to the highest value in their range (1.25v). The software reads the DE memory location containing the channel that is on (hit), the 128-bit value read, should contain only the one bit that is on. More than one bit on indicates crosstalk. The DAC value is then lowered 1 LSB (5mv) and the DE memory is read again, this repeats until the DAC output is reduced to 150mv. The software then shifts the pattern in the TSM memory one bit so that the next channel is being stimulated with a large amplitude signal, the process of reading the DE memory and lowering the DAC values is repeated. The shifting continues until all 128 channels have been stimulated. Crosstalk is reported each time a nonstimulated channel is on. This procedure shows that channels not responding to the

signals on other channels have less than 3% crosstalk.(Refer to section 5.4.7 PC Crosstalk test).

ACCEPTANCE-The signal amplitude of the input should be set to 500mv peak to peak differential amplitude. The PC module is unacceptable if crosstalk is found on any channel.

SCOTT HOLM 5/8/91

APPENDIX B - FASTBUS INTERFACE PAL PROGRAM

This appendix contains the information on the programming of the EPM5128 PAL that is used for the FASTBUS interface on the POSTAMP/COMPARATOR printed circuit board.

MAX+PLUS Compiler Report File
 Version 2.50 05/31/90

** Design compiled without errors

Title: PA/CMP FASTBUS INTERFACE
 Company: Fermilab
 Designer: KEN TREPTOW
 Rev: E
 Date: 3:06p 11-15-1990
 Turbo: ON
 Security: OFF

B B B B B I I I I G M O O O R
 A A A A A V I I I G M O S S S E
 D D D D D C A E W N S D S S S A
 4 3 2 1 0 S C S G T D 2 K 0 1 2 /

	/	9	8	7	6	5	4	3	2	1	68	67	66	65	64	63	62	61		
BAD5	:	10																	60	STROBE
BAD6	:	11																	59	LDCNTR/
BAD7	:	12																	58	RDCNTR/
BAD8	:	13																	57	OAK
BAD9	:	14																	56	RUN
BAD21	:	15																	55	ENIC
GND	:	16																	54	VCC
BAD22	:	17																	53	ENSC
BAD23	:	18																	52	CCLKEN/
BAD24	:	19																	51	SEL0/
VCC	:	20																	50	GND
BAD30	:	21																	49	SEL1/
BAD31	:	22																	48	SEL2/
IGA0	:	23																	47	SEL3/
IGA1	:	24																	46	DACRD
IGA2	:	25																	45	SW2
IGA3	:	26																	44	SW1
			27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	

I I I C S I G I I I V D D D D N N
 G A N L W A N R M M C N N N N T T
 A D V K 0 K D D S S C T T T T A A
 4 1 A 1 0 1 A A A A 1 0
 8 D O N 5 4 3 2

** RESOURCE USAGE **

ic Array Block	Macrocells	I/O Pins	Expanders	External Interconnect
A: MC1 - MC16	15/16(93%)	8/ 8(100%)	27/32(84%)	19/24(79%)
B: MC17 - MC32	7/16(43%)	5/ 5(100%)	11/32(34%)	19/24(79%)
C: MC33 - MC48	4/16(25%)	5/ 5(100%)	1/32(3%)	6/24(25%)
D: MC49 - MC64	15/16(93%)	8/ 8(100%)	0/32(0%)	11/24(45%)
E: MC65 - MC80	16/16(100%)	8/ 8(100%)	15/32(46%)	23/24(95%)
F: MC81 - MC96	6/16(37%)	5/ 5(100%)	15/32(46%)	17/24(70%)
G: MC97 - MC112	7/16(43%)	5/ 5(100%)	3/32(9%)	24/24(100%)
H: MC113 - MC128	16/16(100%)	8/ 8(100%)	12/32(37%)	23/24(95%)

Total dedicated input pins used: 8/ 8 (100%)
 Total I/O pins used: 52/ 52 (100%)
 Total macrocells used: 86/128 (67%)
 Total expanders used: 84/256 (32%)

Total input pins required: 20
 Total output pins required: 24
 Total bidirectional pins required: 16
 Total macrocells required: 86
 Total expanders in database: 69

Synthesized macrocells: 0/128 (0%)

** FILE HIERARCHY **

```
! DACMAP: 78!  
! DACMAP: 78! 74139: 28!  
! DACMAP: 78! 74151: 30!  
! DACMAP: 78! 74151: 18!  
! DACMAP: 78! 74151: 17!  
! DACMAP: 78! 74151: 16!  
! DACMAP: 78! 74151: 15!  
! DACMAP: 78! 74151: 5!  
! NTAREG: 48!  
! NTAREG: 48! DACSEL: 108!  
! NTAREG: 48! DACSEL: 108! 74138H: 11!  
! NTAREG: 48! CT8: 93!  
! CONTROL: 45!  
! CONTROL: 45! DELAY: 165!  
! GASEL: 46!  
! OUTMUX: 50!  
! OUTMUX: 50! 74153: 81!  
! OUTMUX: 50! 74138H: 82!  
! OUTMUX: 50! 74153: 74!  
! OUTMUX: 50! 74153: 75!  
! OUTMUX: 50! 74153: 76!  
! OUTMUX: 50! 74153: 77!  
! OUTMUX: 50! 74153: 78!  
!   TMUX: 50! 74153: 79!  
!   TMUX: 50! 74153: 80!  
! CSR0: 49!
```

** INPUTS **

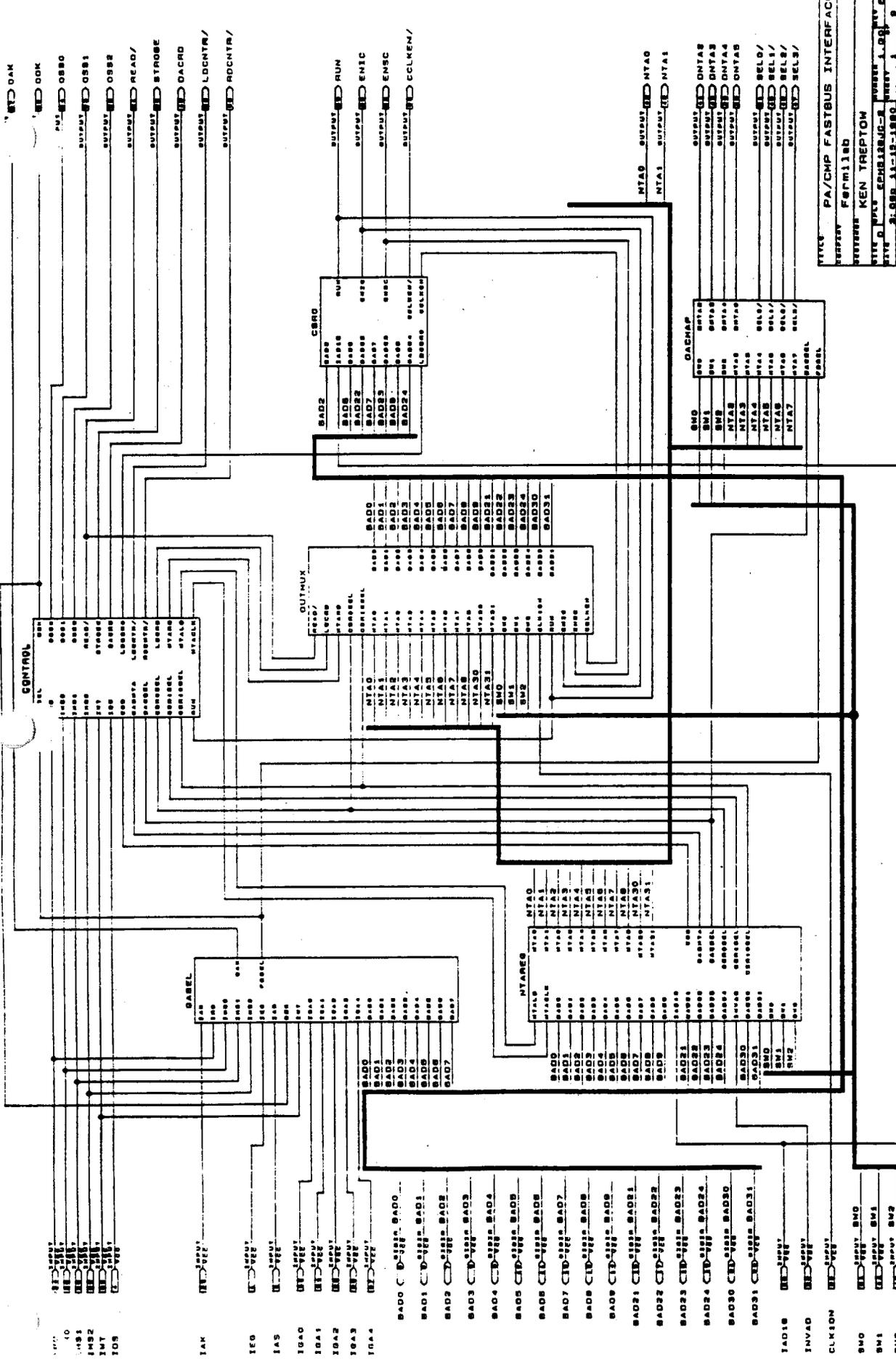
	MCell	LAB	Primitive	Expanders		Fan-In		Name
				Total	Shared	INP	FBK	
7			INPUT	0	0	0	0	BAD0
5	(2)	(A)	INPUT	0	0	0	0	BAD1
6	(3)	(A)	INPUT	0	0	0	0	BAD2
7	(4)	(A)	INPUT	0	0	0	0	BAD3
8	(5)	(A)	INPUT	0	0	0	0	BAD4
9	(6)	(A)	INPUT	0	0	0	0	BAD5
10	(7)	(A)	INPUT	0	0	0	0	BAD6
11	(8)	(A)	INPUT	0	0	0	0	BAD7
12	(17)	(B)	INPUT	0	0	0	0	BAD8
13	(18)	(B)	INPUT	0	0	0	0	BAD9
14	(19)	(B)	INPUT	0	0	0	0	BAD21
15	(20)	(B)	INPUT	0	0	0	0	BAD22
17	(21)	(B)	INPUT	0	0	0	0	BAD23
18	(33)	(C)	INPUT	0	0	0	0	BAD24
19	(34)	(C)	INPUT	0	0	0	0	BAD30
21	(35)	(C)	INPUT	0	0	0	0	BAD31
22	(36)	(C)	INPUT	0	0	0	0	CLK10N
30	(55)	(D)	INPUT	0	0	0	0	IAD18
28	(53)	(D)	INPUT	0	0	0	0	IAK
32	-	-	INPUT	0	0	0	0	IAS
2	-	-	INPUT	0	0	0	0	IDS
4	(1)	(A)	INPUT	0	0	0	0	IEG
1	-	-	INPUT	0	0	0	0	IGA0
23	(37)	(C)	INPUT	0	0	0	0	IGA1
24	(49)	(D)	INPUT	0	0	0	0	IGA2
25	(50)	(D)	INPUT	0	0	0	0	IGA3
6	(51)	(D)	INPUT	0	0	0	0	IGA4
27	(52)	(D)	INPUT	0	0	0	0	IMS0
35	-	-	INPUT	0	0	0	0	IMS1
36	-	-	INPUT	0	0	0	0	IMS2
66	-	-	INPUT	0	0	0	0	INVAD
29	(54)	(D)	INPUT	0	0	0	0	IRD
34	-	-	INPUT	0	0	0	0	IWT
68	-	-	INPUT	0	0	0	0	SW0
31	(56)	(D)	INPUT	0	0	0	0	SW1
44	(71)	(E)	INPUT	0	0	0	0	SW2
45	(72)	(E)	INPUT	0	0	0	0	

** OUTPUTS **

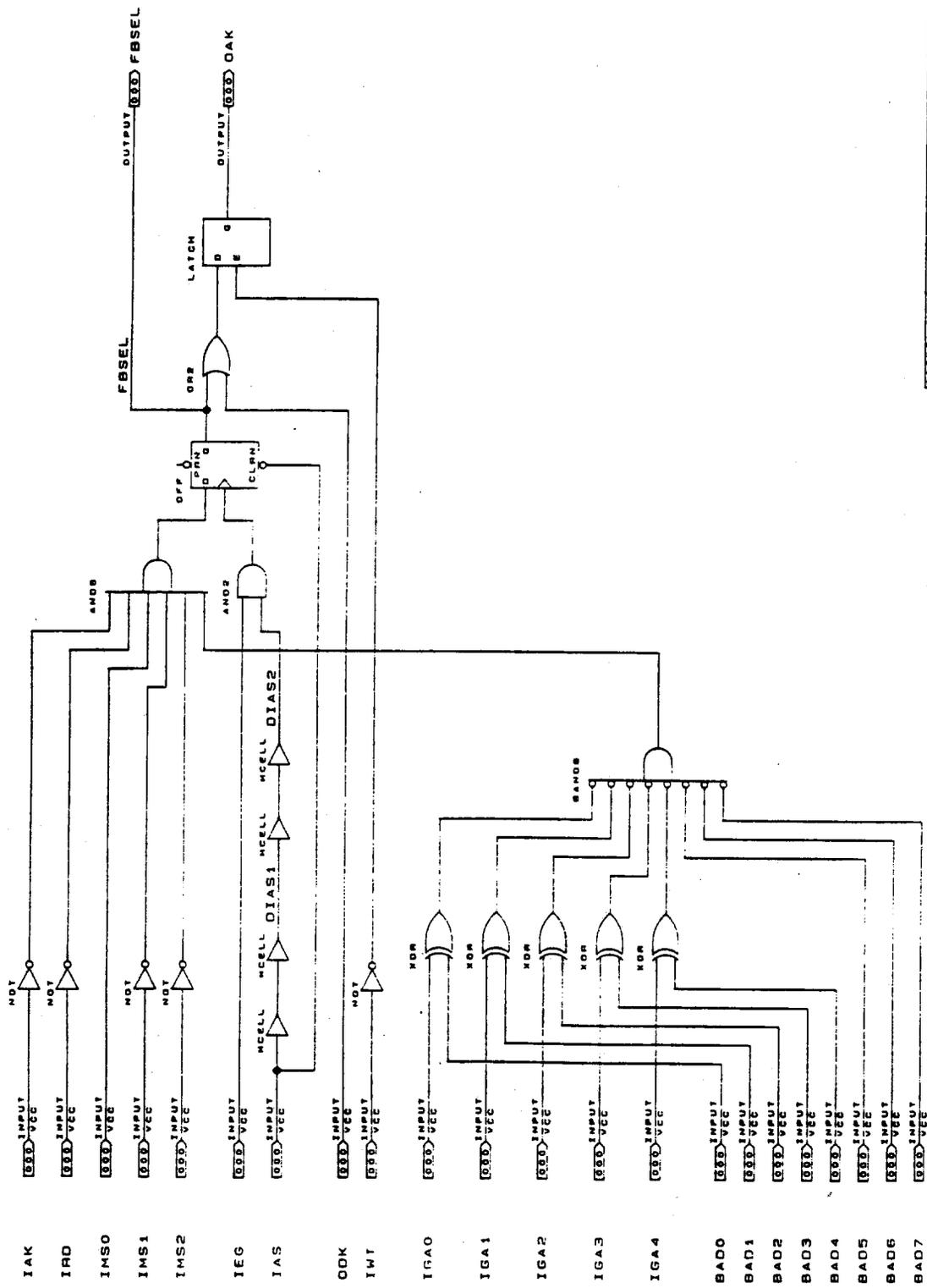
n	MCell	LAB	Primitive	Expanders		Fan-In		Name
				Total	Shared	INP	FBK	
5	2	A	OR4	11	11	7	14	BAD0
6	3	A	OR4	11	11	7	14	BAD1
7	4	A	OR4	11	11	7	15	BAD2
8	5	A	OR4	11	11	7	14	BAD3
9	6	A	OR4	11	11	7	15	BAD4
10	7	A	OR4	11	11	7	14	BAD5
11	8	A	OR4	11	11	7	15	BAD6
12	17	B	OR4	11	11	4	15	BAD7
13	18	B	OR4	1	1	4	6	BAD8
14	19	B	OR4	1	1	5	4	BAD9
15	20	B	OR4	1	1	4	4	BAD21
17	21	B	OR4	1	1	4	2	BAD22
18	33	C	OR4	1	1	4	4	BAD23
19	34	C	OR4	1	1	4	4	BAD24
21	35	C	OR4	1	1	4	5	BAD30
22	36	C	OR4	1	1	4	5	BAD31
52	97	G	MCELL	0	0	0	1	CCLKEN/
46	81	F	OUTPUT	0	0	4	7	DACRD
41	68	E	OUTPUT	0	0	3	1	DNTA2
40	67	E	OUTPUT	0	0	3	2	DNTA3
39	66	E	OUTPUT	0	0	3	3	DNTA4
38	65	E	OUTPUT	5	0	3	4	DNTA5
55	99	G	DFE	3	3	6	15	ENIC
53	98	G	DFE	3	3	6	15	ENSC
59	114	H	OUTPUT	0	0	4	15	LDCNTR/
3	70	E	DFE	0	0	1	3	NTA0
2	69	E	DFE	0	0	1	4	NTA1
57	101	G	LATCH	0	0	1	2	OAK
65	120	H	LATCH	0	0	1	2	ODK
64	119	H	OUTPUT	0	0	3	3	OSS0
63	118	H	OUTPUT	8	7	4	11	OSS1
62	117	H	OUTPUT	7	7	4	10	OSS2
58	113	H	OUTPUT	0	0	3	13	RDCNTR/
61	116	H	OUTPUT	0	0	4	2	READ/
56	100	G	DFE	3	3	6	15	RUN
51	85	F	OUTPUT	5	0	3	11	SEL0/
49	84	F	OUTPUT	3	0	3	11	SEL1/
48	83	F	OUTPUT	4	0	3	11	SEL2/
47	82	F	OUTPUT	3	0	3	11	SEL3/
60	115	H	OUTPUT	0	0	3	10	STROBE

** BURIED LOGIC **

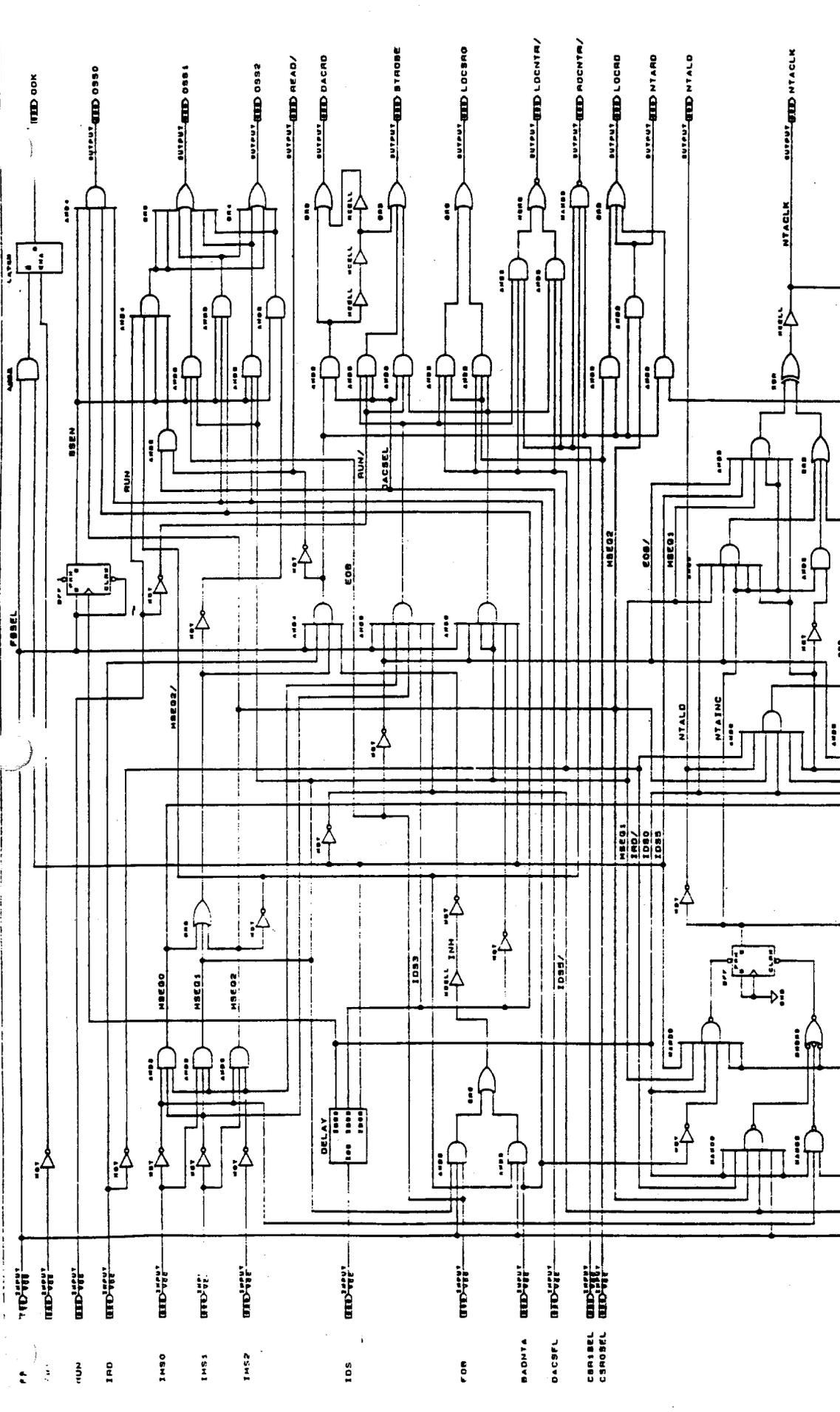
	MCell	LAB	Primitive	Expanders		Fan-In		Name
				Total	Shared	INP	FBK	
-	64	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 IDS0
-	63	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 IDS1
-	62	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 IDS2
-	61	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 IDS3
-	60	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 IDS4
-	80	E	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 IDS5
-	57	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 :34
(27)	52	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 :37
-	59	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 :38
-	58	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 :39
(31)	56	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 :41
(30)	55	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 :42
-	79	E	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 :43
(29)	54	D	MCELL	0	0	1	0	:CONTROL:45 DELAY:165 :46
(26)	51	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 :49
(25)	50	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 :50
-	128	H	MCELL	0	0	3	3	:CONTROL:45 INH
-	78	E	MCELL	0	0	3	6	:CONTROL:45 NTACLK
-	77	E	MCELL	0	0	4	5	:CONTROL:45 NTACLK0/2
-	76	E	DFE	3	0	4	5	:CONTROL:45 NTAINC
-	96	F	DFE	0	0	0	2	:CONTROL:45 SSEN
-	16	A	MCELL	0	0	4	6	:CONTROL:45 :187
-	15	A	MCELL	0	0	0	1	:CONTROL:45 :188
-	14	A	MCELL	0	0	0	1	:CONTROL:45 :189
-	127	H	DFE	3	3	6	15	:CSR0:49 CCLKEN
-	13	A	MCELL	0	0	0	1	:GASEL:46 DIAS1
-	112	G	MCELL	0	0	0	1	:GASEL:46 DIAS2
-	75	E	DFE	7	0	20	1	:GASEL:46 FBSEL
-	12	A	MCELL	0	0	1	0	:GASEL:46 :21
-	111	G	MCELL	0	0	0	1	:GASEL:46 :51
-	126	H	MCELL	0	0	0	12	:NTAREG:48 BADNTA
-	31	B	DFE	0	0	1	5	:NTAREG:48 CT8:93 Q2
-	74	E	DFE	0	0	1	6	:NTAREG:48 CT8:93 Q3
-	73	E	DFE	0	0	1	7	:NTAREG:48 CT8:93 Q4
(45)	72	E	DFE	0	0	1	8	:NTAREG:48 CT8:93 Q5
(44)	71	E	DFE	0	0	1	9	:NTAREG:48 CT8:93 Q6
-	125	H	DFE	0	0	1	10	:NTAREG:48 CT8:93 Q7
-	11	A	SOFT	7	0	3	6	:NTAREG:48 DACSEL:108 :52
-	10	A	SOFT	7	0	3	8	:NTAREG:48 DACSEL:108 :53
-	124	H	MCELL	0	0	0	13	:NTAREG:48 EN/
-	123	H	DFE	1	0	0	15	:NTAREG:48 EOB
(28)	53	D	DFE	0	0	8	2	:NTAREG:48 NTA8
-	122	H	DFE	0	0	1	2	:NTAREG:48 NTA30
-	121	H	DFE	0	0	1	2	:NTAREG:48 NTA31
-	9	A	SOFT	2	0	4	13	:OUTMUX:50 :90
-	32	B	SOFT	0	0	4	12	:OUTMUX:50 :91



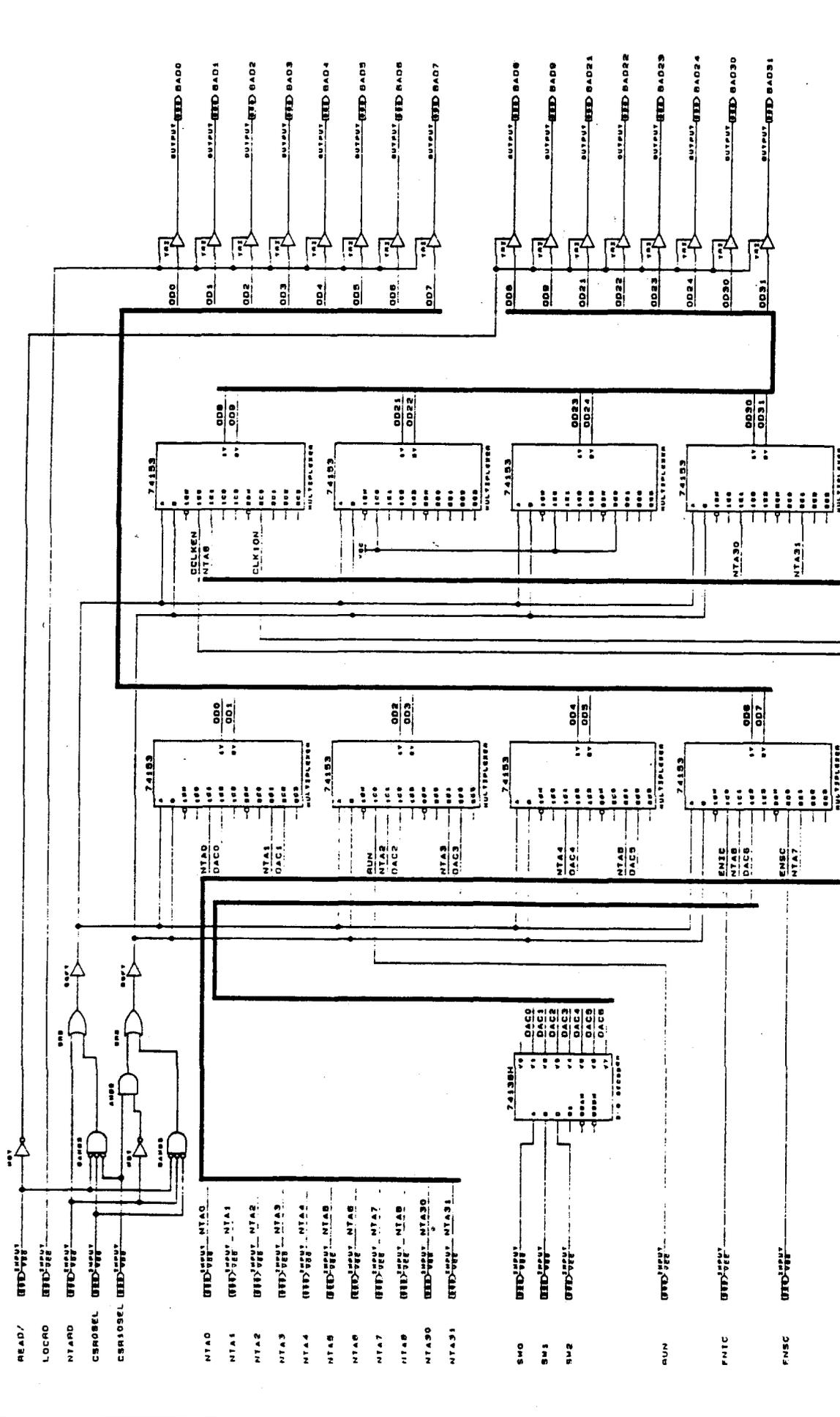
TITLE PA/CMP FASTBUS INTERFACE
 NUMBER 1001110
 DESIGNER KEN TREPTON
 CITY DALLAS
 DATE 3-28-88 11:43-AM
 DRAWN 1-08
 CHECKED 1-08
 SECURITY OFF



TITLE	PA/CMP FB GA SEL LOGIC
COMPANY	FERMILAB
DESIGNER	KEN TREPTOW
SITE C	EPUS EPM5128
DATE	5/11/90
NUMBER	1.00
REV	B
YOURS	5/11/90
BY	9
SECURITY	OFF

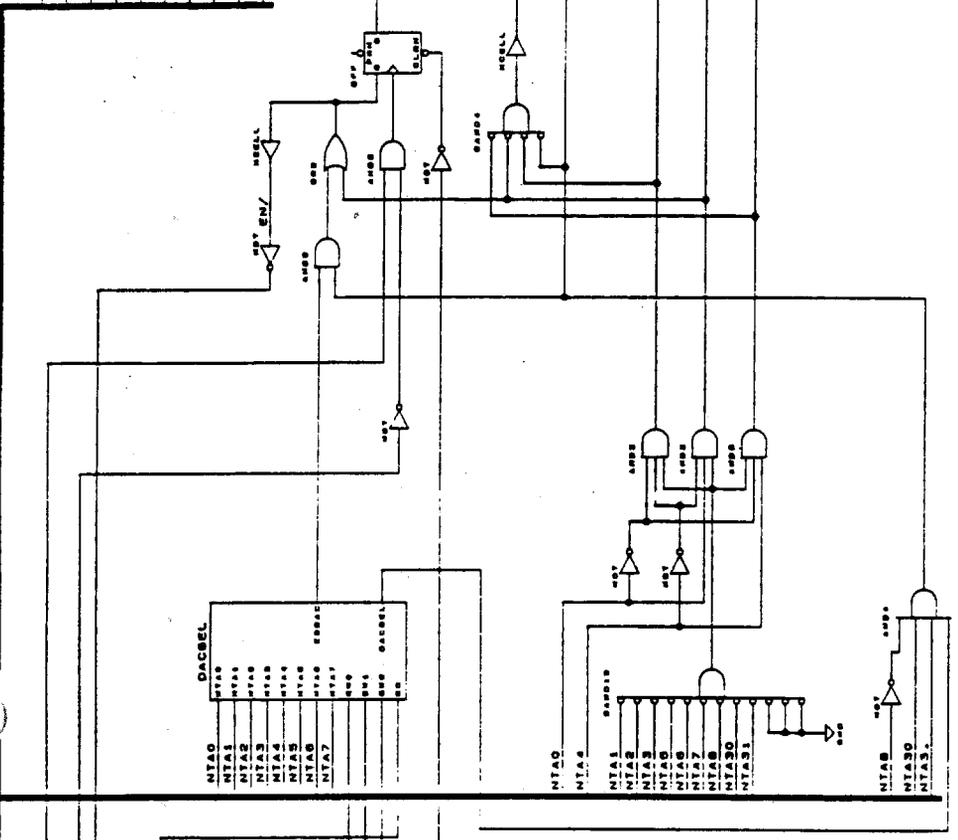


PA/CMP CONTROL LOGIC
 FORM 118B
 KEN TREPTON
 18-188-AD-17-1880
 SECURITY OF



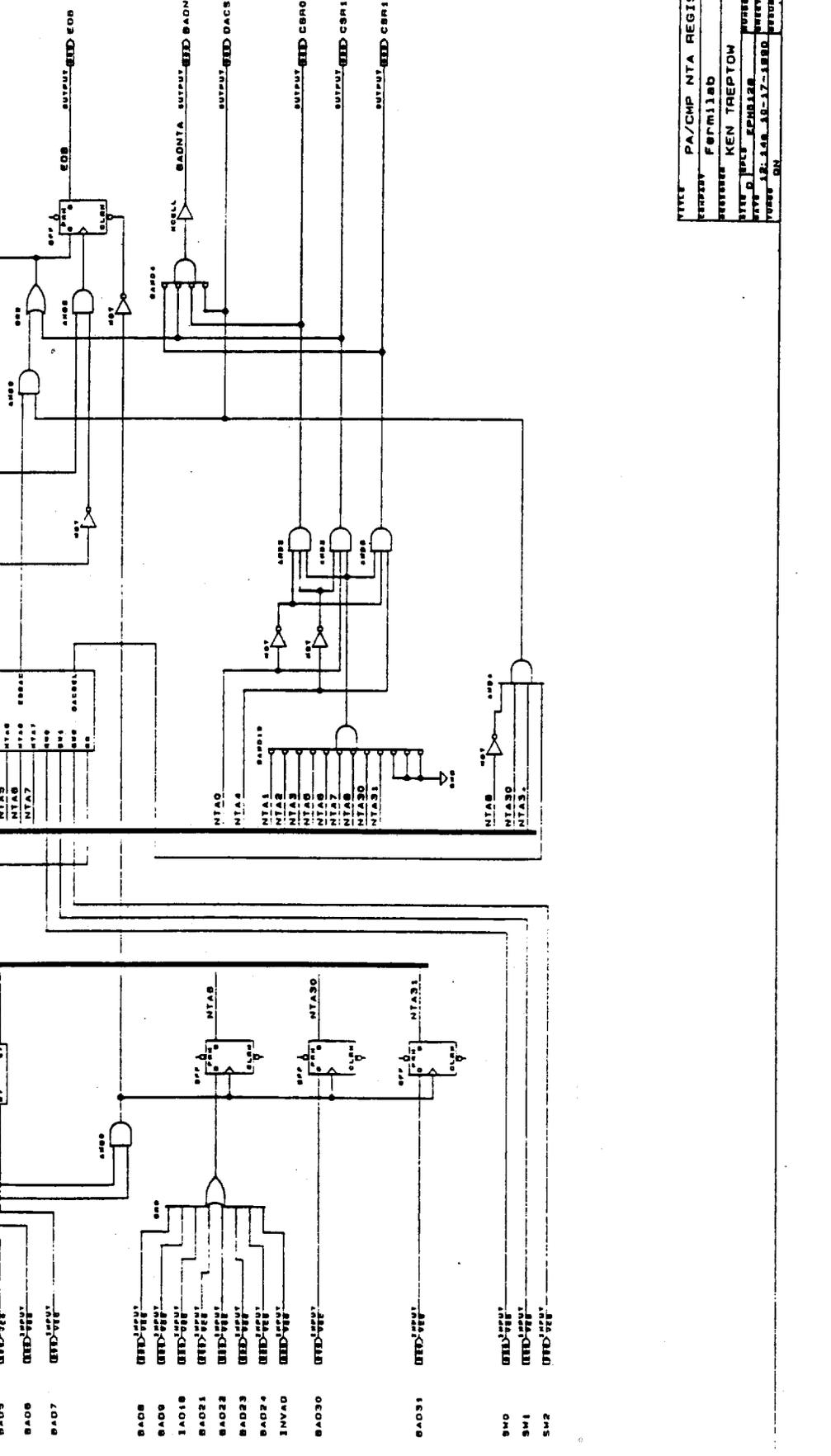
PA/CMP OUTPUT MUX
 PROPERTY FERMILAB
 DESIGNED BY KEN TREPTON
 DATE 01/25/82
 DRAWN BY J. G. BERRY
 CHECKED BY J. G. BERRY
 REVISION 9
 SHEET 9 OF 9

NTA0 D NTA0
 NTA1 INPUT EED NTA1
 NTA2 INPUT EED NTA2
 NTA3 INPUT EED NTA3
 NTA4 OUTPUT EED NTA4
 NTA5 INPUT EED NTA5
 NTA6 INPUT EED NTA6
 NTA7 INPUT EED NTA7
 NTA8 INPUT EED NTA8
 NTA9 INPUT EED NTA9
 NTA10 INPUT EED NTA10
 NTA11 INPUT EED NTA11
 NTA12 INPUT EED NTA12
 NTA13 INPUT EED NTA13



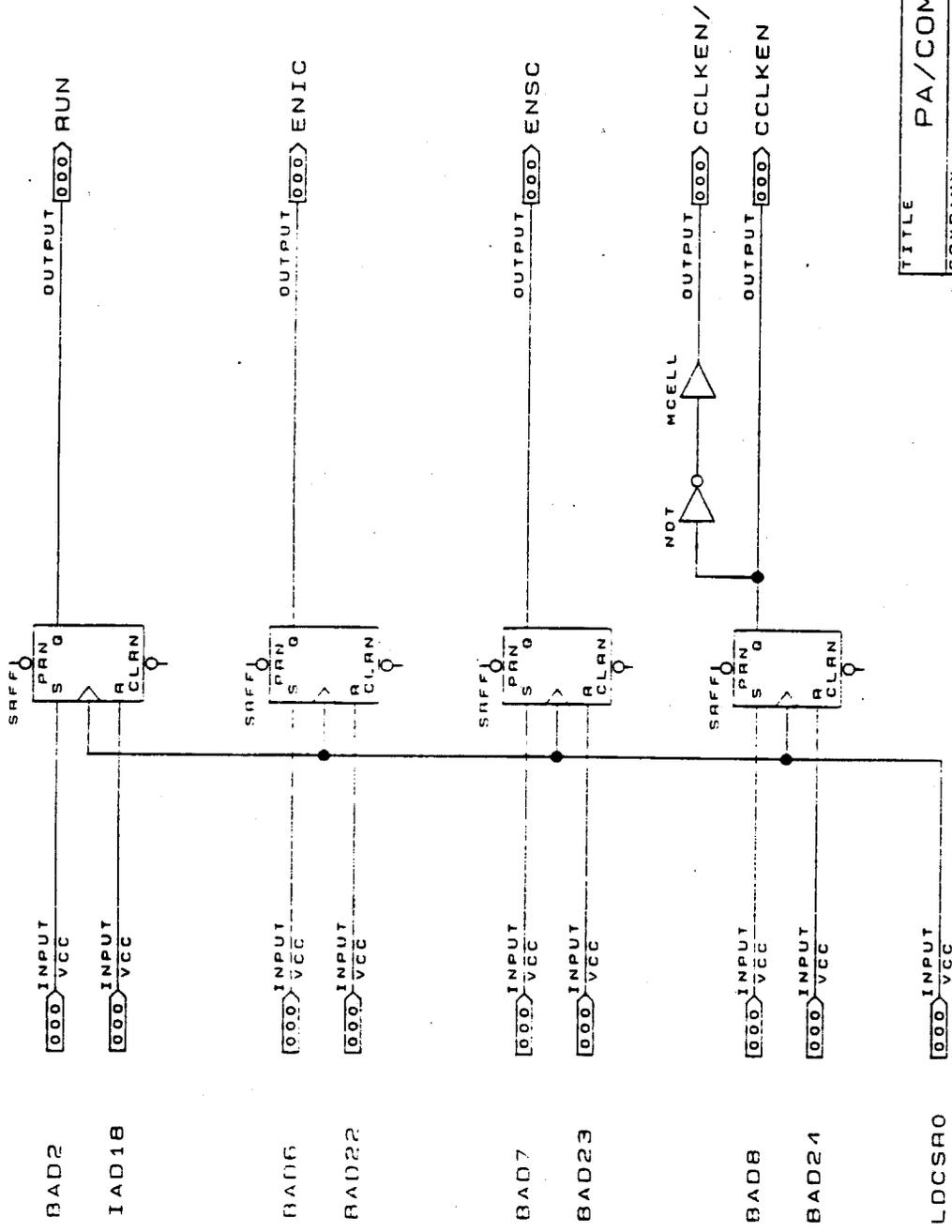
NTA0 DATA EN
 NTA1 DATA EN
 NTA2 DATA EN
 NTA3 DATA EN
 NTA4 DATA EN
 NTA5 DATA EN
 NTA6 DATA EN
 NTA7 DATA EN
 NTA8 DATA EN
 NTA9 DATA EN
 NTA10 DATA EN
 NTA11 DATA EN
 NTA12 DATA EN
 NTA13 DATA EN

NTA0 OUTPUT EED NTA0
 NTA1 OUTPUT EED NTA1
 NTA2 OUTPUT EED NTA2
 NTA3 OUTPUT EED NTA3
 NTA4 OUTPUT EED NTA4
 NTA5 OUTPUT EED NTA5
 NTA6 OUTPUT EED NTA6
 NTA7 OUTPUT EED NTA7
 NTA8 OUTPUT EED NTA8
 NTA9 OUTPUT EED NTA9
 NTA10 OUTPUT EED NTA10
 NTA11 OUTPUT EED NTA11
 NTA12 OUTPUT EED NTA12
 NTA13 OUTPUT EED NTA13

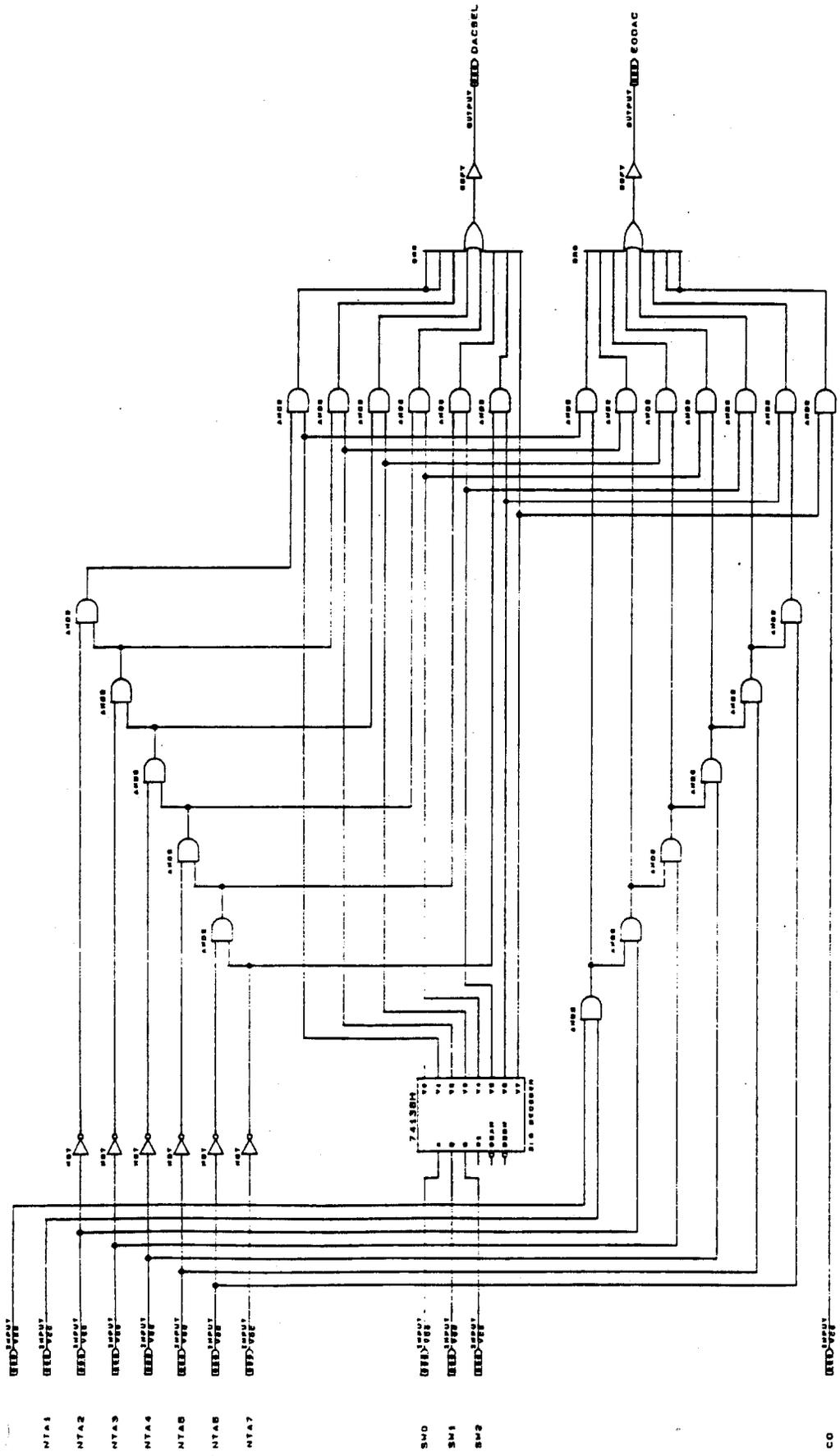


PA/CMP NTA REGISTER
 FORM 1180
 KEN TREPTOW
 10-17-1980

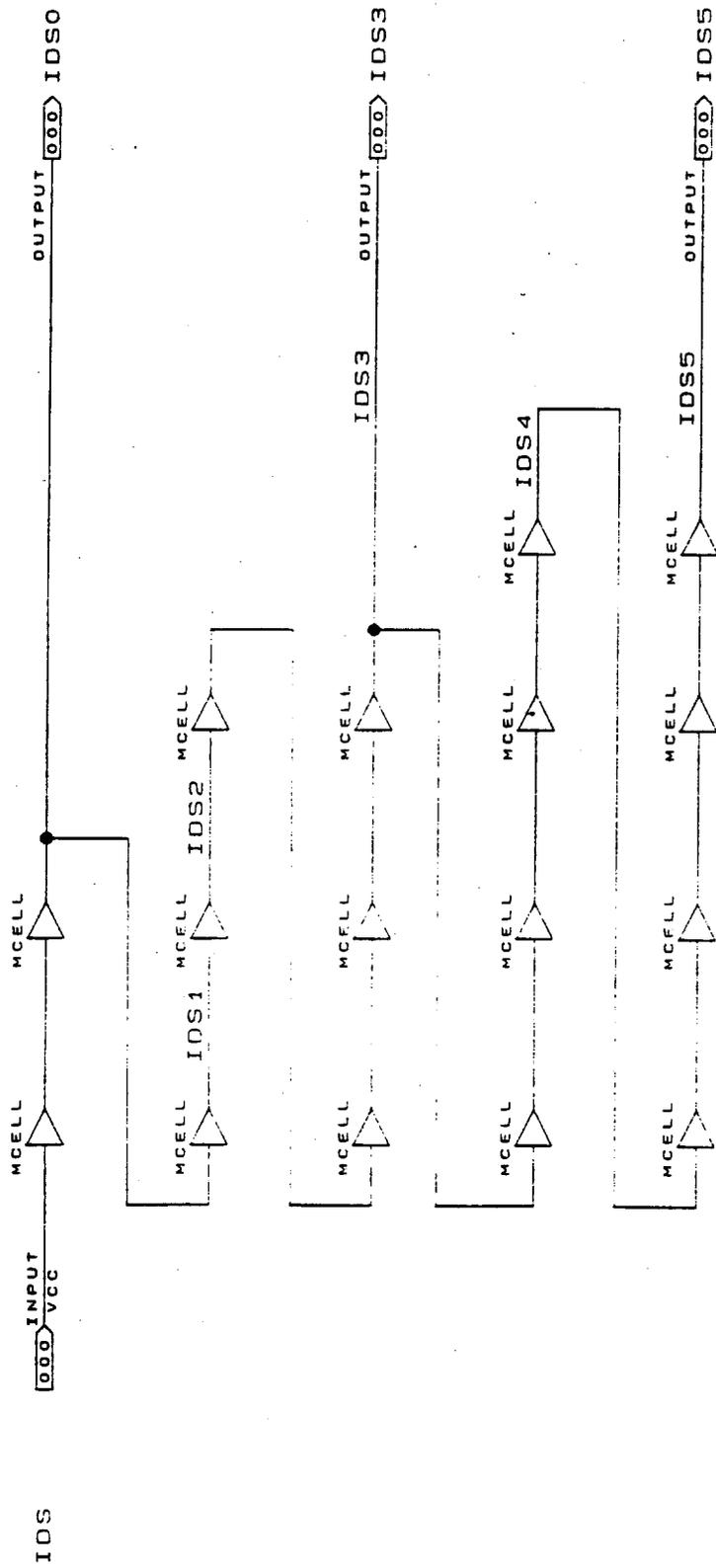
REVISION 1
 DATE 10-17-1980
 BY KEN TREPTOW
 CHECKED BY [Blank]
 APPROVED BY [Blank]
 TITLE PA/CMP NTA REGISTER



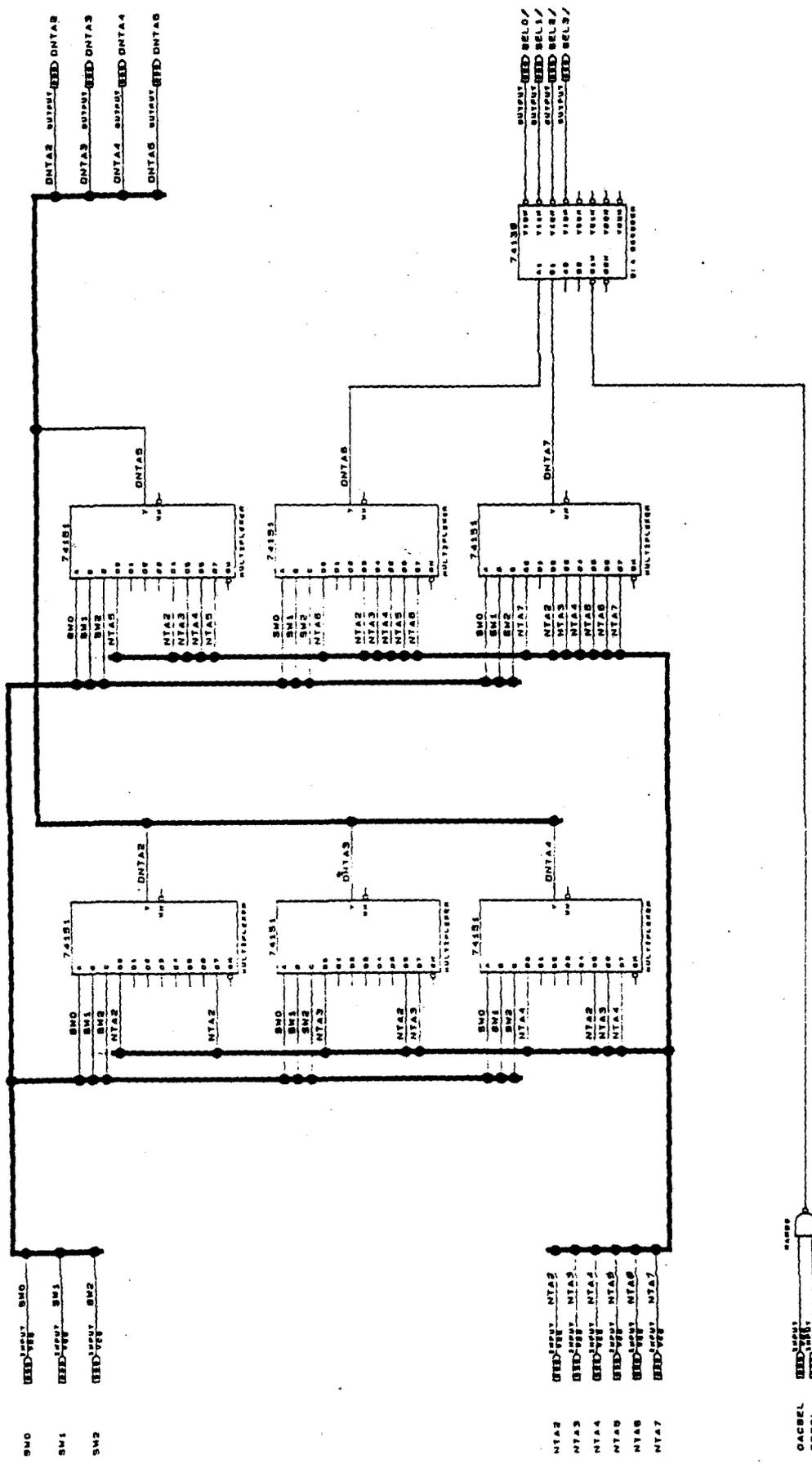
TITLE		PA/COMP CSRO	
COMPANY		FERMILAB/CD/DAE	
DESIGNER		KEN TREPTOW	
SIZE	EPLO	NUMBER	1.00
DATE	6/26/90	SHEET	6 OF 9
TURBO	ON	SECURITY	OFF



TITLE PA/CMP DAC ADDR DECODE
 DESIGN F87M180
 DESIGNER KEN TREPTON
 DATE 11/13/88
 DRAWN 1-08/88
 CHECKED 12-17-88
 SECURITY OFF



TITLE	PA/CMP DS DELAYS		
COMPANY	Fermilab		
DESIGNER	KEN TREPTOW		
SIZE	8	EPLD	EP5128
DATE	10:22a 11-13-1990		NUMBER 1.00 REV A
TURBO	ON	SECURITY	OFF
		SHEET	8 OF 9



TITLE PA/CMP DAC MAPPING LOGI
 NUMBER F8M118B/CO/DAE
 DESIGNED BY KEN TREPTON
 DATE 10/19/80
 DRAWN BY J. B. B. 11-18-1980
 CHECKED BY J. B. B. 11-18-1980
 SECURITY OFF

GACBEL
 FBSEL

3.5 HARDWARE JUMPERS

3.5.1 DAC/ADC Jumpers

The illustration is an abbreviated pattern of the IC-03 DAC/ADC jumpering scheme which exists on the P/C Module.

There are 256 DACs which are addressed via CSR addresses C000_0000 through C000_00FF inclusive. DAC address 00 (Hex), will always set the threshold voltage on the uppermost trace which is the threshold for the discriminator connected to the output of the summed channel which takes the sum of channel -1 and channel 0 ($\Sigma-1,0$). Likewise DAC address 01 (Hex), will always set the threshold voltage on the trace immediately below the uppermost trace which is the threshold for the discriminator connected directly to the individual channel #0 input. DAC address 02 (Hex), will always set the threshold voltage for the discriminator connected to the output of the summed channel which takes the sum of channel 0 and channel 1 ($\Sigma 0,1$). DAC address 03 (Hex), will always set the threshold voltage for the discriminator connected directly to the individual channel #1 input. This pattern continues for the 256 DACs and the 256 discriminator threshold setting inputs.

It should be obvious that if all 256 DAC's are employed, no jumpers are required and each discriminator has an individual DAC to control it's threshold. However, in the event that only 4 of the 256 DAC's are mounted on the P/C Module, the jumpers would probably be applied such that DAC 00 (hex) would drive every other sum channel. i.e., $\Sigma(0)$, $\Sigma(1,2)$, $\Sigma(3,4)$, $\Sigma(5,6)$ etc. DAC 01 (hex) would drive the even individual channels; DAC 02 (hex) would drive sum channels $\Sigma(0,1)$, $\Sigma(2,3)$, $\Sigma(4,5)$, $\Sigma(6,7)$ etc., and DAC 03 (hex) would drive the odd, individual channels.

The common choices of DAC populations are 4,8,16,32,64,128 or 256 which corresponds to 1,2,4,8,16,32 and 64 IC-03 packages. It seems reasonable to assume that for four DAC's every fourth threshold lead would be connected together and so on. However, any and all possibilities exist for connecting DAC outputs to threshold inputs and the method used may be dictated by the detector geometry.

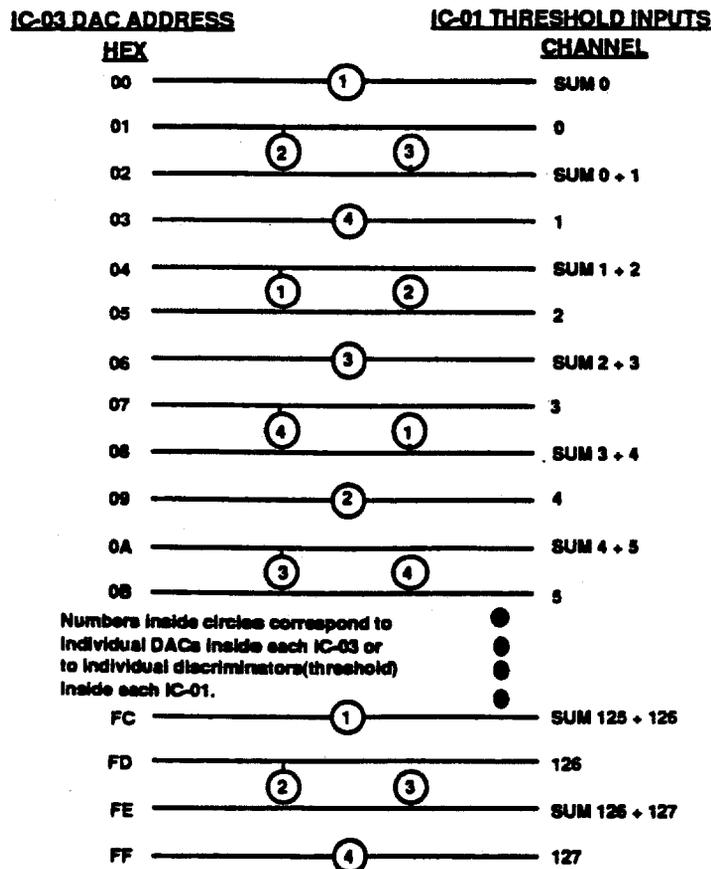


Figure 21: DAC/ADC Jumpering

3.5.2 CSR10 Jumpers

The value found in CSR10 corresponds to the configuration of three, two position jumpers(JU2, JU3, and JU4) that connect a signal trace to ground(GND) or +5V. The physical module location of the three posts for each jumper, and their connections are shown below. Table 1 on the following page provides the relationship between DAC population, jumper location, CSR10 readback and lowest ordered address for each DAC chip.

When less than 256 DAC's are utilized, the P/C module will be populated from the lowest address onward without skipping addresses, this is done by a mapping routine within the EPM5128 programmable PAL. It has been done this way to make the DACs accessible by block transfer. The PAL receives a 3 bit code from the jumpers to indicate the number of IC-03 DAC/ADC chips mounted and covers the sequential DAC address it receives from an external source to the appropriate DAC module address. I.E. if only two IC-03s(8 DACs) are used and located at DAC board address 0 through 3(U97) and DAC board address 64 through 67(U129), the PAL knowing from the jumpering scheme will only accept DAC addresses 0 through 7 from an external source and in turn converts external address 0 to DAC board address 0 and so on up to external address 7 to DAC board address 67. When less than 256 DACs are employed the IC-03s physical location is important to insure that the external address received is converted to the appropriate DAC board address. The physical locations for the common number of IC-03s used are shown in Table 2 on the following page.

CSR10 JUMPERING DIAGRAM

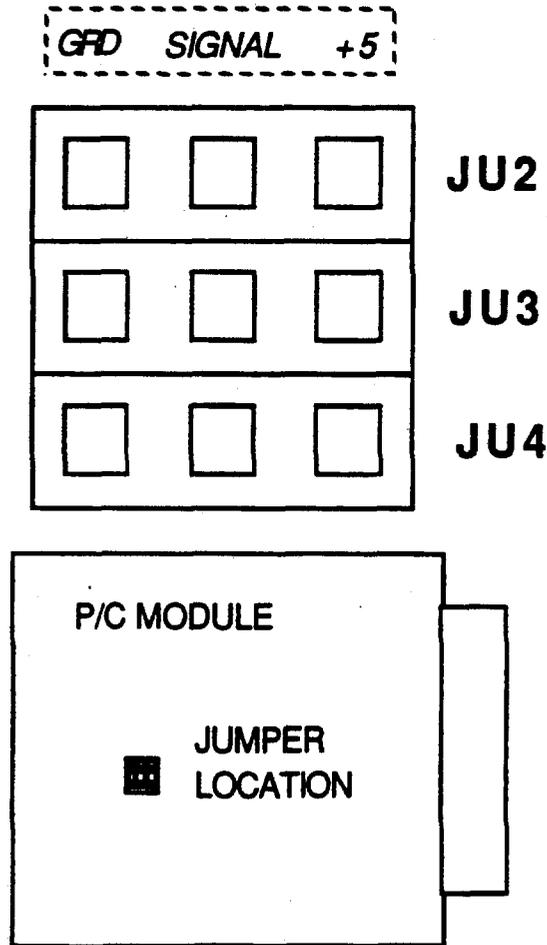


Figure 22: CSR10 Jumpering

Table 1

Jumper Numbers			# of DACs	CSR10 Value	First DAC board address of each IC-03
JU2	JU3	JU4			
Gnd	Gnd	Gnd	????	0	This is a special case, unique to the user.
Gnd	Gnd	+5V	4	1	0
Gnd	+5V	Gnd	8	2	0,80
Gnd	+5V	+5V	16	4	0,40,80,C0
+5V	Gnd	Gnd	32	8	0,20,40,60,80,A0,C0,E0
+5V	Gnd	+5 V	64	10	0,10,20,30,40,50,60,70,80,90,A0,B0,C0,D0,E0,F0
+5V	+5V	Gnd	128	20	0,8,10,18,20,28,30,38,40,48,50,58,60,68,70,7880,88,90,98,A0,A8,B0,B8,C0,C8,D0,D8,E0,E8, F0,F8
+5V	+5V	+5V	256	40	All addresses from 00 through FF inclusive are valid

Table 2

Number of IC-03s mounted(#DACs)	IC-03 Physical location on module
1(4)	U97
2(8)	U97, U129
4(16)	U97, U113, U129, U145
8(32)	U97, U105, U113, U121, U129, U137, U145, U153
16(64)	U97, U101, U105, U109, U113, U117, U121, U125, U129, U133, U137, U141, U145, U149, U153, U157
32(128)	U97, U99, U101, U103, U105, U107, U109, U111, U113, U115, U117, U119, U121, U123, U125, U127, U129, U131, U133, U135, U137, U139, U141, U143, U145, U147, U149, U151, U153, U155, U157, U159
64(256)	ALL LOCATIONS

4.0 P/C MODULE - TESTING AND CALIBRATION

4.1 UNPOWERED TEST

A test should be performed to check for shorts between the power planes (layers) of the P/C module. The test should verify no direct connection between any of the following power planes: -5.2V, -3.5V, -2V, -.8V top, -.8V bottom, +5V, +3.5V, +1.25V, and ground. The test can be done with an OHM METER. Connection to the power plane can be found at the following locations, with the measured impedances between the power and ground plane with the PC board fully assembled (number of IC-03s equals four).

-5.2V = right side of D5	= 8 ohm
-3.5V = right side of fuse f4	= 3 ohm
-2V = right side of fuse f1	= 22 ohm
-.8V top = right side of CR2	= 23 ohm
-.8V bottom = right side of CR4	= 23 ohm
+5V = right side of fuse f6	= 400 ohm(90 ohm with EPM5128 installed)
153 = right side of fuse f2	= 580 ohm
+1.25V = case of Q1	= 73 ohm
GROUND = left side of D5	

NOTE: Right side is towards the front of the board where the LABEL is located. The drawing "POWER TEST POINT DETAILS"#2563.000-MD-215808 shows the power pin locations of various devices on the top side of the board, this should help in finding shorts.

4.2 AUTOMATED TESTING

There is an "Acceptance Test Description" document that uses two software packages to verify whether a P/C module is acceptable from an outside vendor. This document can be found in APPENDIX A.

4.3 CALIBRATION

Adjusting the value at which the **TEMP** LED on the front panel of the P/C module will turn on is the only calibration needed for the module. Adjusting trim pot R295 sets the temperature at which the LED will turn on and off, the setting of R295 controls the voltage on pin 2 of U185. If pin 3 of U185 which is connected to the LM35 temperature sensor is at a more positive value than pin 2 of U185 the LED will turn on. The voltage on pin 2 should be set to 0.5V this corresponds to 50 degrees Celsius. The LM35 will output to pin 3 of the U185 a 10 mV per degree Celsius voltage level. If the temperature rises above 50 degrees Celsius(0.5V on pin 3) the LED will turn on. The LED will turn off if the temperature falls below 50 degrees Celsius. The **TEMP** LED and associated circuitry can be tested by adjusting R295 for a voltage on pin 2 of U185 that is less than the value on pin 3 of U185, the lower voltage should cause the **TEMP** LED to turn on.

5.0 APPENDICES

- APPENDIX A - TEST SOFTWARE**
- APPENDIX B - FASTBUS INTERFACE PAL PROGRAM**
- APPENDIX C - POSTAMP/COMPARATOR MODULE - SCHEMATIC**
- APPENDIX D - MODULE DRAWINGS**
- APPENDIX E - DATA SHEETS**

APPENDIX A - TEST SOFTWARE

This appendix contains an acceptance criteria specification that pertains to the testing of the POSTAMP/COMPARATOR printed circuit board.

POSTAMP/COMPARATOR MODULE - ACCEPTANCE TEST DESCRIPTION

The party performing the acceptance test on the POSTAMP/COMPARATOR module should be familiar with the "IEEE Standard FASTBUS Modular High-Speed Data Acquisition and Control system"(ANSI/IEEE Std. 960-1986), the POSTAMP/COMPARATOR HARDWARE DESCRIPTION-HN100, and the two software packages listed below which the acceptance criteria is based upon. Questions pertaining to the documents should be addressed to the appropriate originator.

SILICON STRIP DETECTOR (SSD)

System Test Software Guide

Version: 0 15 march 1991

Originators:

Wolfgang Kowald Duke University

EXP.771 #708-840-4250

Panagiotis Spentzouris UCA

EXP.771 #708-840-4250

Dave Slimmer Fermilab

Computing Dept. #708-840-4334

SILICON STRIP DETECTOR SYSTEM "SINGLE BOARD DIAGNOSTICS TESTS"-PN434

Software Description

Version: 1 4/25/91

Originator:

Garry R. Moore Fermilab

Computing Dept. #708-840-4059

POSTAMP/COMPARATOR HARDWARE DESCRIPTION-HN100

Complete Module Documentation Manual

Version: 3 5/7/91

Originators:

Merle Haldeman Fermilab

RD/DEG group #708-840-3958

Scott Holm Fermilab

RD/DEG group #708-840-4340

Bruce Merkel Fermilab

RD/DEG group #708-840-3263

In order for the PC module to be accepted, the PC module must pass the following four tests.

1. PC TEST

Refer to the "SINGLE BOARD DIAGNOSTICS TESTS" documentation listed above.

PC_TEST is a menu driven software tool capable of effectively testing and/or exercising all FASTBUS accessible circuitry of the POSTAMP/COMPARATOR module. The test should be run in the "Exercise Postamp Comparator" mode; this is #3 under the PC_TEST main menu. This option will fully exercise all FASTBUS accessible circuitry of the PC module including all geographical address, secondary address, and DAC/ADC circuitry.

ACCEPTANCE- The software will respond with errors if the module responds incorrectly. The module is unacceptable when any errors are reported.

EXCEPTIONS: A part of the test writes and then reads a series of IC-03 DAC values, the software will respond with an error if the DAC value read back is more than plus or minus one LSB different than the written value. The module however, will be accepted when the DAC value read back is within two LSB's of the written value.

Refer to the "SILICON STRIP DETECTOR (SSD)" documentation listed on page 1 for the remaining three tests.

2. PC test counter test

This test uses an 8-bit counter on the PC module to generate 256 patterns used for testing the output portion(IC-02 and IC-04 ASIC's) of the PC module. The 8-bit counter cycles through 256 output pattern possibilities which are sent to the IC-02 and IC-04 test inputs; t1 and t2. The outputs of the IC-02s and IC-04s provide 256 different 128-bit patterns which are sent to the DE module through the FASTBUS auxiliary backplane. This test effectively tests the outputs of all IC-02 and IC-04 ASIC's as well as their connections to the backplane. The DE module has 256 memory locations which are continually being loaded with the 256 pattern possibilities. In this test an individual DE memory location is always being loaded with the same pattern generated by the PC module test counter.(Refer to section 5.4.2 PC test counter test and to APPENDIX A for test counter patterns).

ACCEPTANCE- The PC module is acceptable if no errors occur. The software will know in which memory location in the DE module each pattern generated by PC module's IC-02 and IC-04 ASICs are stored. When a memory location in the DE module is read by the software, the 128-bit pattern in that location is compared with the 128-bit pattern that was expected for that location. An error is reported if the values do not match.

3. PC channel characterization tests

This test characterizes individual and sum channel threshold voltage sensitivity for the PC module discriminator electronics. Characterizing a channel involves placing a test signal at a channel input and then scanning through the threshold setting DAC, value range with the software recording the highest threshold voltage(DAC value) at which the channel discriminator was able to detect the input test signal. The test should be performed in the default mode(DAC vs CHANNEL mode). In this mode, five separate routines need to be run on the module. These routines are listed in a menu that is displayed after "PC channel characterization test"(h) is selected from the System test menu. Invoking any one of the routines, automatically sets up the PC module for that

routine, i.e. turning on individual channel or sum channel mode, and placing the PC module in the RUN mode.

The first routine, "INDIVIDUAL CHANNEL", tests all individual channels of the PC module. The software performs in the following way: the TSM module's 256 word by 128 bit memory (refer to TSM document#) is loaded with a pattern of alternating words consisting of all A's and 5's, which means adjacent bits in a given word have opposite values as well as a given bit in adjacent memory addresses. The TSM module feeds this pattern to the LS module (refer to LS module documentation#) which continually places this pattern at the PC module input. The DE continuously updates its 256 memory locations with the 128-bit pattern that the PC module outputs through the FASTBUS auxiliary backplane. At the start, all DACs are set to the highest value in their range (1.25v) and at some instance the software performs 8 nonconsecutive reads of a DE memory location, recording which if any of the 128 channels were on (hit) during each of the 8 reads. The DAC value is then lowered 1 LSB (5mv) and the DE module memory is read 8 more times, this continues until the DACs are at their lowest value in their range (0mv). A graph is made that shows the DAC values at which a channel responded to 8 out of 8 reads with the channel on (hit) and also when the channel responds at least once but less than 8 out of 8 times.

The remaining four routines test the SUM channels. Each routine uses a different pattern such as 1's, 2's, 4's or 8's, i.e. for the 2's pattern every 2nd channel of a 4 channel combination will be toggling on and for the 8's pattern every 4th channel of a 4 channel combination will be toggling on. A graph is made for each routine. In the SUM channel mode when placing an input signal on one channel the adjacent channels also receive this input signal, therefore the adjacent channels should also turn on and the graphs should reflect this. (Refer to section 5.4.6 PC Channel Characterization Tests).

ACCEPTANCE- The input signal from the LS module should be set for a 40mv peak to peak differential amplitude. The PC module passes the test if the resulting graphs that are produced by the software are as follows. **{SHOW GRAPHS}** The DAC values of all channels may vary no more than plus or minus 15 counts from the norm, i.e. if the norm is at the DAC value of 90, acceptable DAC values range from 75 to 105. A module is unacceptable if a channel is characterized outside of the plus or minus 15 count range.

4. PC Crosstalk Test

PC Crosstalk test will test the ability of the PC module to reject crosstalk to other channels from an input signal of substantial amplitude on a certain other channel. The Crosstalk test uses the TSM and LS modules as in the PC characterization test. In this test the TSM memory is loaded with a 1 in one of the 128 bits of the first word and the remaining 255 words have a 0 in all 128 bits. This means that 1 channel is being stimulated with a 18.9ns pulse every 4.8us. The TSM module feeds this pattern to the LS module which continuously places the pattern at the PC module input, meanwhile the DE is continuously updating its 256 memory locations with the 128-bit pattern that the PC module outputs through the FASTBUS auxiliary backplane. Initially, all DACs are set to the highest value in their range (1.25v). The software reads the DE memory location containing the channel that is on (hit), the 128-bit value read, should contain only the one bit that is on. More than one bit on indicates crosstalk. The DAC value is then lowered 1 LSB (5mv) and the DE memory is read again, this repeats until the DAC output is reduced to 150mv. The software then shifts the pattern in the TSM memory one bit so that the next channel is being stimulated with a large amplitude signal, the process of reading the DE memory and lowering the DAC values is repeated. The shifting continues until all 128 channels have been stimulated. Crosstalk is reported each time a nonstimulated channel is on. This procedure shows that channels not responding to the

signals on other channels have less than 3% crosstalk.(Refer to section 5.4.7 PC Crosstalk test).

ACCEPTANCE-The signal amplitude of the input should be set to 500mv peak to peak differential amplitude. The PC module is unacceptable if crosstalk is found on any channel.

SCOTT HOLM 5/8/91

APPENDIX B - FASTBUS INTERFACE PAL PROGRAM

This appendix contains the information on the programming of the EPM5128 PAL that is used for the FASTBUS interface on the POSTAMP/COMPARATOR printed circuit board.

MAX+PLUS Compiler Report File
 Version 2.50 05/31/90

** Design compiled without errors

Title: PA/CMP FASTBUS INTERFACE
 Company: Fermilab
 Designer: KEN TREPTOW
 Rev: E
 Date: 3:06p 11-15-1990
 Turbo: ON
 Security: OFF

B B B B B I I I I I G M O O O O R
 A A A A A I V I I I G M O S S S S A
 D D D D D D C A E W N S D S S S D
 4 3 2 1 0 S C S G T D 2 K 0 1 2 /

	/	9	8	7	6	5	4	3	2	1	68	67	66	65	64	63	62	61		
BAD5	:	10																	60	STROBE
BAD6	:	11																	59	LDCNTR/
BAD7	:	12																	58	RDCNTR/
BAD8	:	13																	57	OAK
BAD9	:	14																	56	RUN
BAD21	:	15																	55	ENIC
GND	:	16																	54	VCC
BAD22	:	17																	53	ENSC
BAD23	:	18																	52	CCLKEN/
BAD24	:	19																	51	SEL0/
VCC	:	20																	50	GND
BAD30	:	21																	49	SEL1/
BAD31	:	22																	48	SEL2/
IGA0	:	23																	47	SEL3/
IGA1	:	24																	46	DACRD
IGA2	:	25																	45	SW2
IGA3	:	26																	44	SW1
			27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	

I I I C S I G I I I V D D D D N N
 G A N L W A N R M M C N N N N T T
 A D V K 0 K D D S S C T T T T A A
 4 1 A 1 0 1 A A A A 1 0
 8 D O 5 4 3 2
 N

** RESOURCE USAGE **

ic Array Block	Macrocells	I/O Pins	Expanders	External Interconnect
A: MC1 - MC16	15/16(93%)	8/ 8(100%)	27/32(84%)	19/24(79%)
B: MC17 - MC32	7/16(43%)	5/ 5(100%)	11/32(34%)	19/24(79%)
C: MC33 - MC48	4/16(25%)	5/ 5(100%)	1/32(3%)	6/24(25%)
D: MC49 - MC64	15/16(93%)	8/ 8(100%)	0/32(0%)	11/24(45%)
E: MC65 - MC80	16/16(100%)	8/ 8(100%)	15/32(46%)	23/24(95%)
F: MC81 - MC96	6/16(37%)	5/ 5(100%)	15/32(46%)	17/24(70%)
G: MC97 - MC112	7/16(43%)	5/ 5(100%)	3/32(9%)	24/24(100%)
H: MC113 - MC128	16/16(100%)	8/ 8(100%)	12/32(37%)	23/24(95%)

Total dedicated input pins used:	8/ 8 (100%)
Total I/O pins used:	52/ 52 (100%)
Total macrocells used:	86/128 (67%)
Total expanders used:	84/256 (32%)

Total input pins required:	20
Total output pins required:	24
Total bidirectional pins required:	16
Total macrocells required:	86
Total expanders in database:	69

Synthesized macrocells:	0/128 (0%)
-------------------------	-------------

** FILE HIERARCHY **

```
! DACMAP: 78!  
! DACMAP: 78! 74139: 28!  
! DACMAP: 78! 74151: 30!  
! DACMAP: 78! 74151: 18!  
! DACMAP: 78! 74151: 17!  
! DACMAP: 78! 74151: 16!  
! DACMAP: 78! 74151: 15!  
! DACMAP: 78! 74151: 5!  
! NTAREG: 48!  
! NTAREG: 48! DACSEL: 108!  
! NTAREG: 48! DACSEL: 108! 74138H: 11!  
! NTAREG: 48! CT8: 93!  
! CONTROL: 45!  
! CONTROL: 45! DELAY: 165!  
! GASEL: 46!  
! OUTMUX: 50!  
! OUTMUX: 50! 74153: 81!  
! OUTMUX: 50! 74138H: 82!  
! OUTMUX: 50! 74153: 74!  
! OUTMUX: 50! 74153: 75!  
! OUTMUX: 50! 74153: 76!  
! OUTMUX: 50! 74153: 77!  
! OUTMUX: 50! 74153: 78!  
!   TMUX: 50! 74153: 79!  
!   TMUX: 50! 74153: 80!  
! CSR0: 49!
```

** INPUTS **

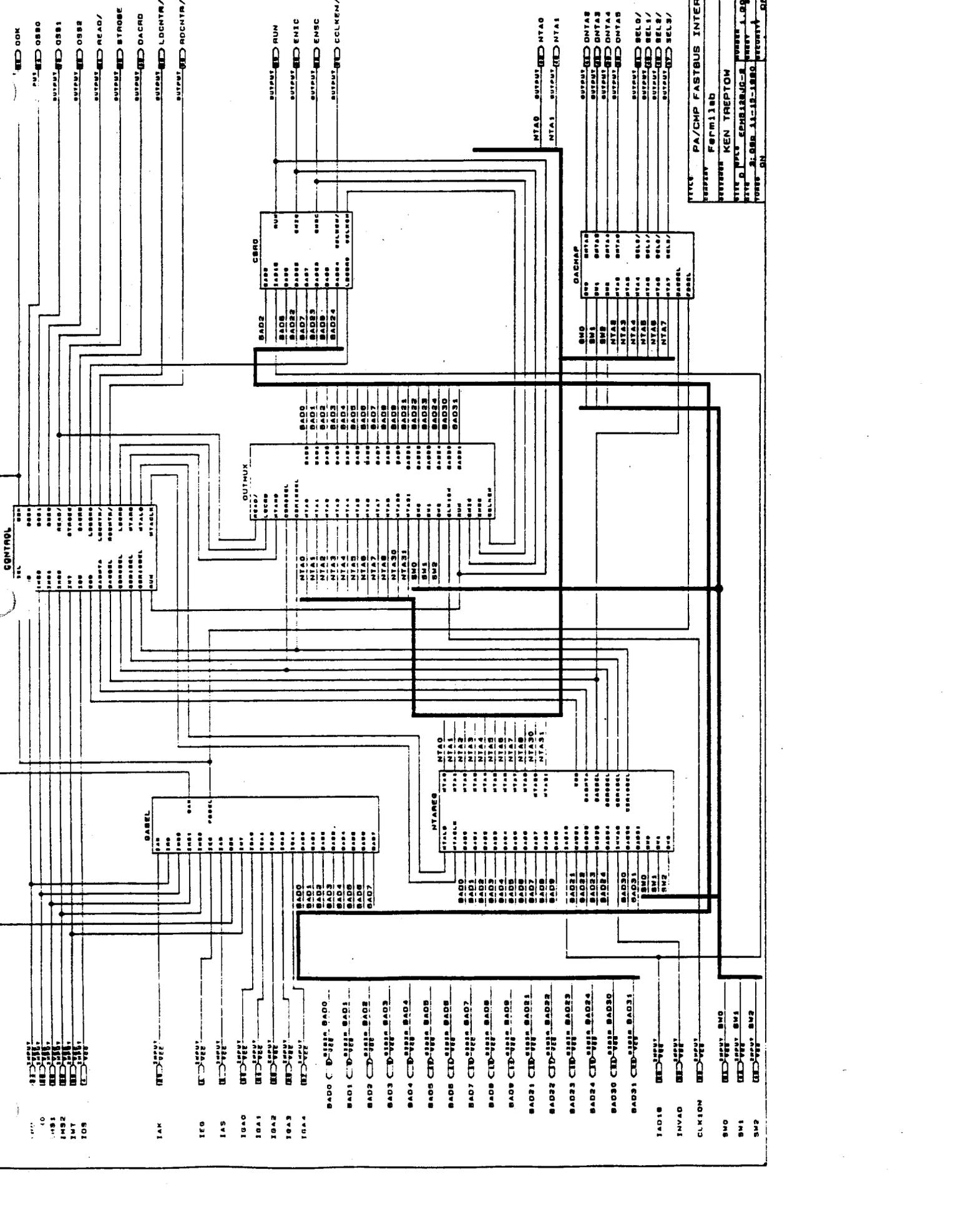
	MCell	LAB	Primitive	Expanders		Fan-In		Name
				Total	Shared	INP	FBK	
7			INPUT	0	0	0	0	BAD0
5	(2)	(A)	INPUT	0	0	0	0	BAD1
6	(3)	(A)	INPUT	0	0	0	0	BAD2
7	(4)	(A)	INPUT	0	0	0	0	BAD3
8	(5)	(A)	INPUT	0	0	0	0	BAD4
9	(6)	(A)	INPUT	0	0	0	0	BAD5
10	(7)	(A)	INPUT	0	0	0	0	BAD6
11	(8)	(A)	INPUT	0	0	0	0	BAD7
12	(17)	(B)	INPUT	0	0	0	0	BAD8
13	(18)	(B)	INPUT	0	0	0	0	BAD9
14	(19)	(B)	INPUT	0	0	0	0	BAD21
15	(20)	(B)	INPUT	0	0	0	0	BAD22
17	(21)	(B)	INPUT	0	0	0	0	BAD23
18	(33)	(C)	INPUT	0	0	0	0	BAD24
19	(34)	(C)	INPUT	0	0	0	0	BAD30
21	(35)	(C)	INPUT	0	0	0	0	BAD31
22	(36)	(C)	INPUT	0	0	0	0	CLK10N
30	(55)	(D)	INPUT	0	0	0	0	IAD18
28	(53)	(D)	INPUT	0	0	0	0	IAK
32	-	-	INPUT	0	0	0	0	IAS
2	-	-	INPUT	0	0	0	0	IDS
4	(1)	(A)	INPUT	0	0	0	0	IEG
1	-	-	INPUT	0	0	0	0	IGA0
23	(37)	(C)	INPUT	0	0	0	0	IGA1
24	(49)	(D)	INPUT	0	0	0	0	IGA2
25	(50)	(D)	INPUT	0	0	0	0	IGA3
6	(51)	(D)	INPUT	0	0	0	0	IGA4
27	(52)	(D)	INPUT	0	0	0	0	IMS0
35	-	-	INPUT	0	0	0	0	IMS1
36	-	-	INPUT	0	0	0	0	IMS2
66	-	-	INPUT	0	0	0	0	INVAD
29	(54)	(D)	INPUT	0	0	0	0	IRD
34	-	-	INPUT	0	0	0	0	IWT
68	-	-	INPUT	0	0	0	0	SW0
31	(56)	(D)	INPUT	0	0	0	0	SW1
44	(71)	(E)	INPUT	0	0	0	0	SW2
45	(72)	(E)	INPUT	0	0	0	0	

** OUTPUTS **

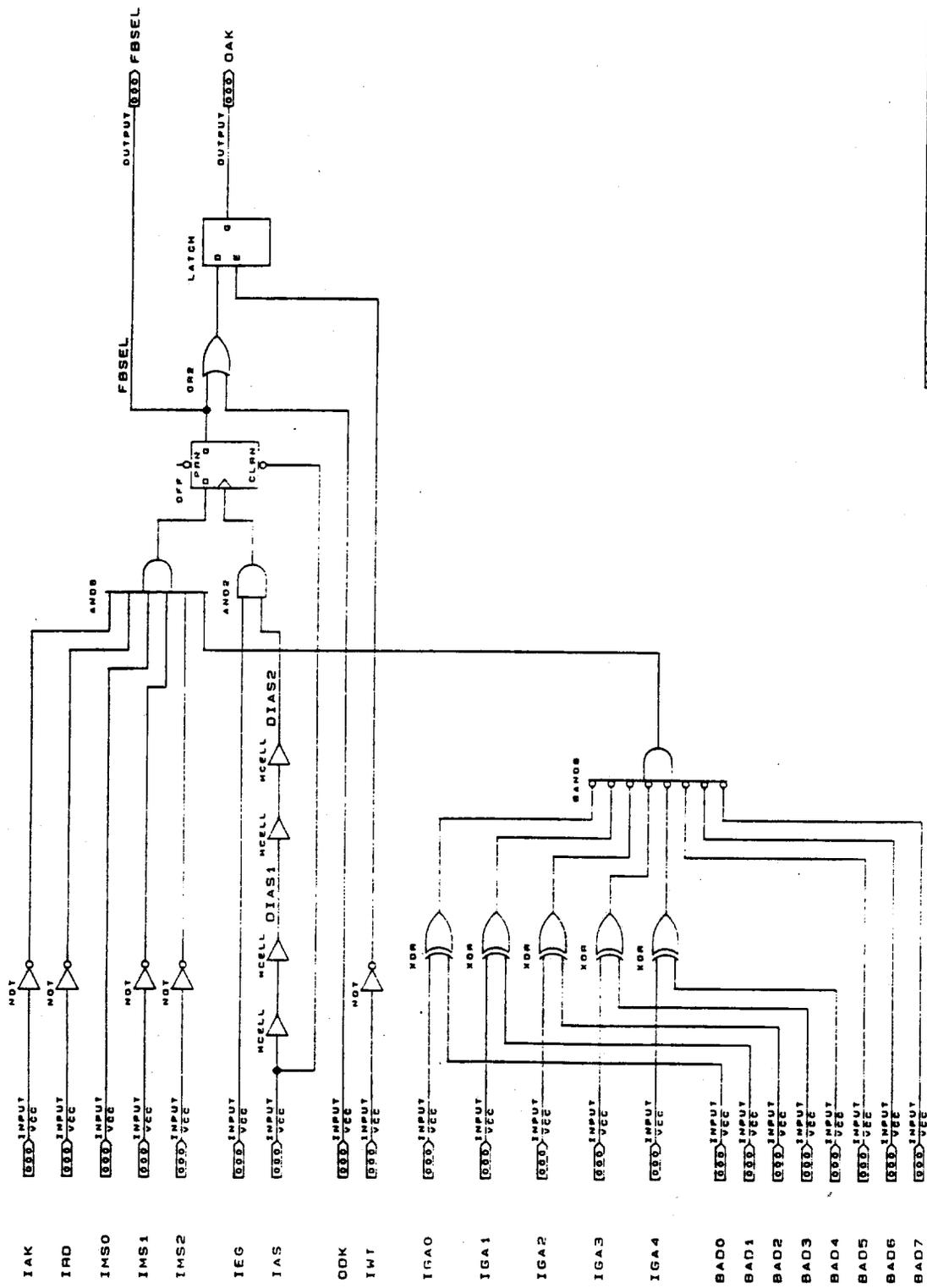
n	MCell	LAB	Primitive	Expanders		Fan-In		Name
				Total	Shared	INP	FBK	
5	2	A	OR4	11	11	7	14	BAD0
6	3	A	OR4	11	11	7	14	BAD1
7	4	A	OR4	11	11	7	15	BAD2
8	5	A	OR4	11	11	7	14	BAD3
9	6	A	OR4	11	11	7	15	BAD4
10	7	A	OR4	11	11	7	14	BAD5
11	8	A	OR4	11	11	7	15	BAD6
12	17	B	OR4	11	11	4	15	BAD7
13	18	B	OR4	1	1	4	6	BAD8
14	19	B	OR4	1	1	5	4	BAD9
15	20	B	OR4	1	1	4	4	BAD21
17	21	B	OR4	1	1	4	2	BAD22
18	33	C	OR4	1	1	4	4	BAD23
19	34	C	OR4	1	1	4	4	BAD24
21	35	C	OR4	1	1	4	5	BAD30
22	36	C	OR4	1	1	4	5	BAD31
52	97	G	MCELL	0	0	0	1	CCLKEN/
46	81	F	OUTPUT	0	0	4	7	DACRD
41	68	E	OUTPUT	0	0	3	1	DNTA2
40	67	E	OUTPUT	0	0	3	2	DNTA3
39	66	E	OUTPUT	0	0	3	3	DNTA4
38	65	E	OUTPUT	5	0	3	4	DNTA5
55	99	G	DFE	3	3	6	15	ENIC
53	98	G	DFE	3	3	6	15	ENSC
59	114	H	OUTPUT	0	0	4	15	LDCNTR/
3	70	E	DFE	0	0	1	3	NTA0
2	69	E	DFE	0	0	1	4	NTA1
57	101	G	LATCH	0	0	1	2	OAK
65	120	H	LATCH	0	0	1	2	ODK
64	119	H	OUTPUT	0	0	3	3	OSS0
63	118	H	OUTPUT	8	7	4	11	OSS1
62	117	H	OUTPUT	7	7	4	10	OSS2
58	113	H	OUTPUT	0	0	3	13	RDCNTR/
61	116	H	OUTPUT	0	0	4	2	READ/
56	100	G	DFE	3	3	6	15	RUN
51	85	F	OUTPUT	5	0	3	11	SEL0/
49	84	F	OUTPUT	3	0	3	11	SEL1/
48	83	F	OUTPUT	4	0	3	11	SEL2/
47	82	F	OUTPUT	3	0	3	11	SEL3/
60	115	H	OUTPUT	0	0	3	10	STROBE

** BURIED LOGIC **

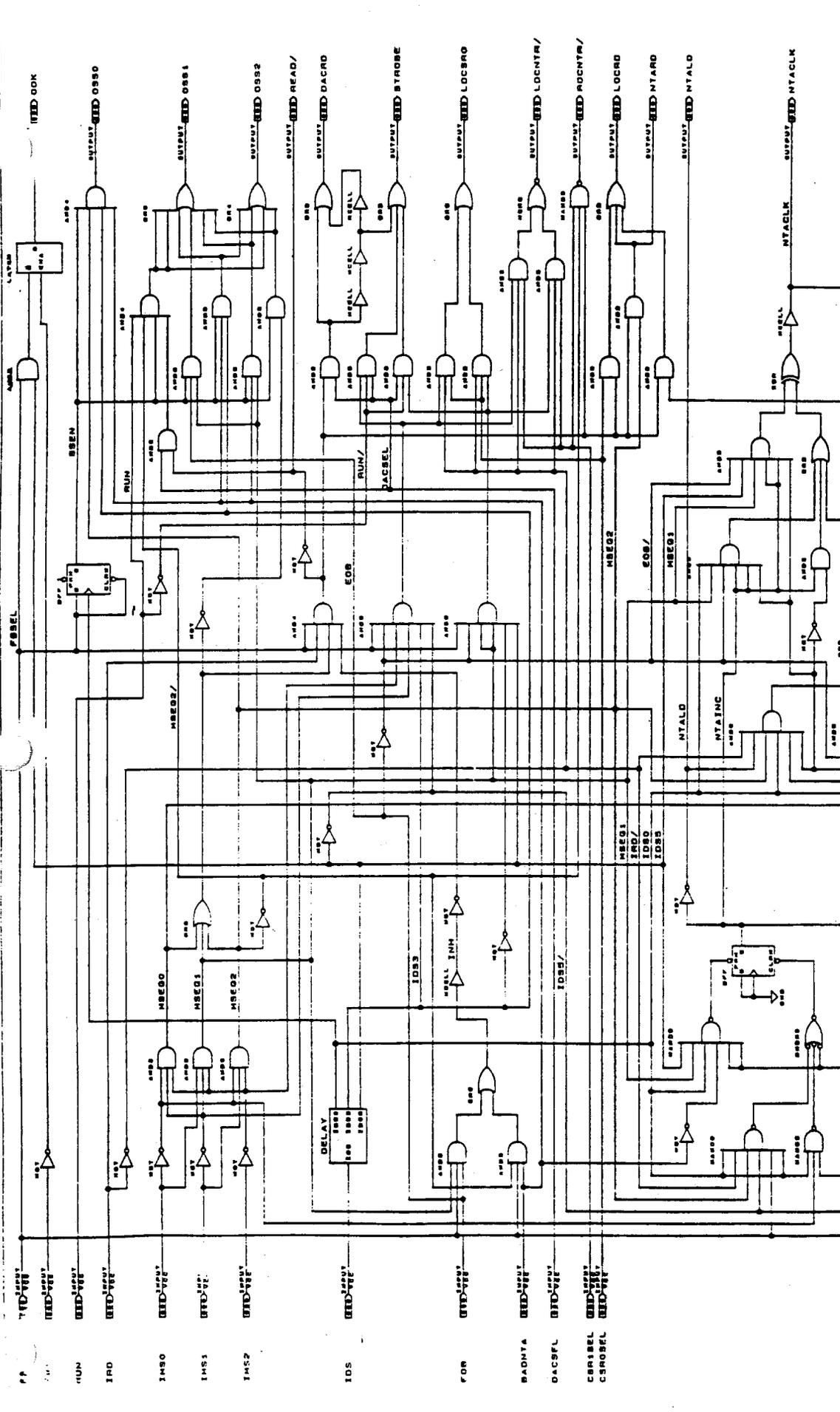
	MCell	LAB	Primitive	Expanders		Fan-In		Name
				Total	Shared	INP	FBK	
-	64	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 IDS0
-	63	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 IDS1
-	62	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 IDS2
-	61	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 IDS3
-	60	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 IDS4
-	80	E	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 IDS5
-	57	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 :34
(27)	52	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 :37
-	59	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 :38
-	58	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 :39
(31)	56	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 :41
(30)	55	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 :42
-	79	E	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 :43
(29)	54	D	MCELL	0	0	1	0	:CONTROL:45 DELAY:165 :46
(26)	51	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 :49
(25)	50	D	MCELL	0	0	0	1	:CONTROL:45 DELAY:165 :50
-	128	H	MCELL	0	0	3	3	:CONTROL:45 INH
-	78	E	MCELL	0	0	3	6	:CONTROL:45 NTACLK
-	77	E	MCELL	0	0	4	5	:CONTROL:45 NTACLK0/2
-	76	E	DFF	3	0	4	5	:CONTROL:45 NTAINC
-	96	F	DFF	0	0	0	2	:CONTROL:45 SSEN
-	16	A	MCELL	0	0	4	6	:CONTROL:45 :187
-	15	A	MCELL	0	0	0	1	:CONTROL:45 :188
-	14	A	MCELL	0	0	0	1	:CONTROL:45 :189
-	127	H	DFF	3	3	6	15	:CSR0:49 CCLKEN
-	13	A	MCELL	0	0	0	1	:GASEL:46 DIAS1
-	112	G	MCELL	0	0	0	1	:GASEL:46 DIAS2
-	75	E	DFF	7	0	20	1	:GASEL:46 FBSEL
-	12	A	MCELL	0	0	1	0	:GASEL:46 :21
-	111	G	MCELL	0	0	0	1	:GASEL:46 :51
-	126	H	MCELL	0	0	0	12	:NTAREG:48 BADNTA
-	31	B	DFF	0	0	1	5	:NTAREG:48 CT8:93 Q2
-	74	E	DFF	0	0	1	6	:NTAREG:48 CT8:93 Q3
-	73	E	DFF	0	0	1	7	:NTAREG:48 CT8:93 Q4
(45)	72	E	DFF	0	0	1	8	:NTAREG:48 CT8:93 Q5
(44)	71	E	DFF	0	0	1	9	:NTAREG:48 CT8:93 Q6
-	125	H	DFF	0	0	1	10	:NTAREG:48 CT8:93 Q7
-	11	A	SOFT	7	0	3	6	:NTAREG:48 DACSEL:108 :52
-	10	A	SOFT	7	0	3	8	:NTAREG:48 DACSEL:108 :53
-	124	H	MCELL	0	0	0	13	:NTAREG:48 EN/
-	123	H	DFF	1	0	0	15	:NTAREG:48 EOB
(28)	53	D	DFF	0	0	8	2	:NTAREG:48 NTA8
-	122	H	DFF	0	0	1	2	:NTAREG:48 NTA30
-	121	H	DFF	0	0	1	2	:NTAREG:48 NTA31
-	9	A	SOFT	2	0	4	13	:OUTMUX:50 :90
-	32	B	SOFT	0	0	4	12	:OUTMUX:50 :91



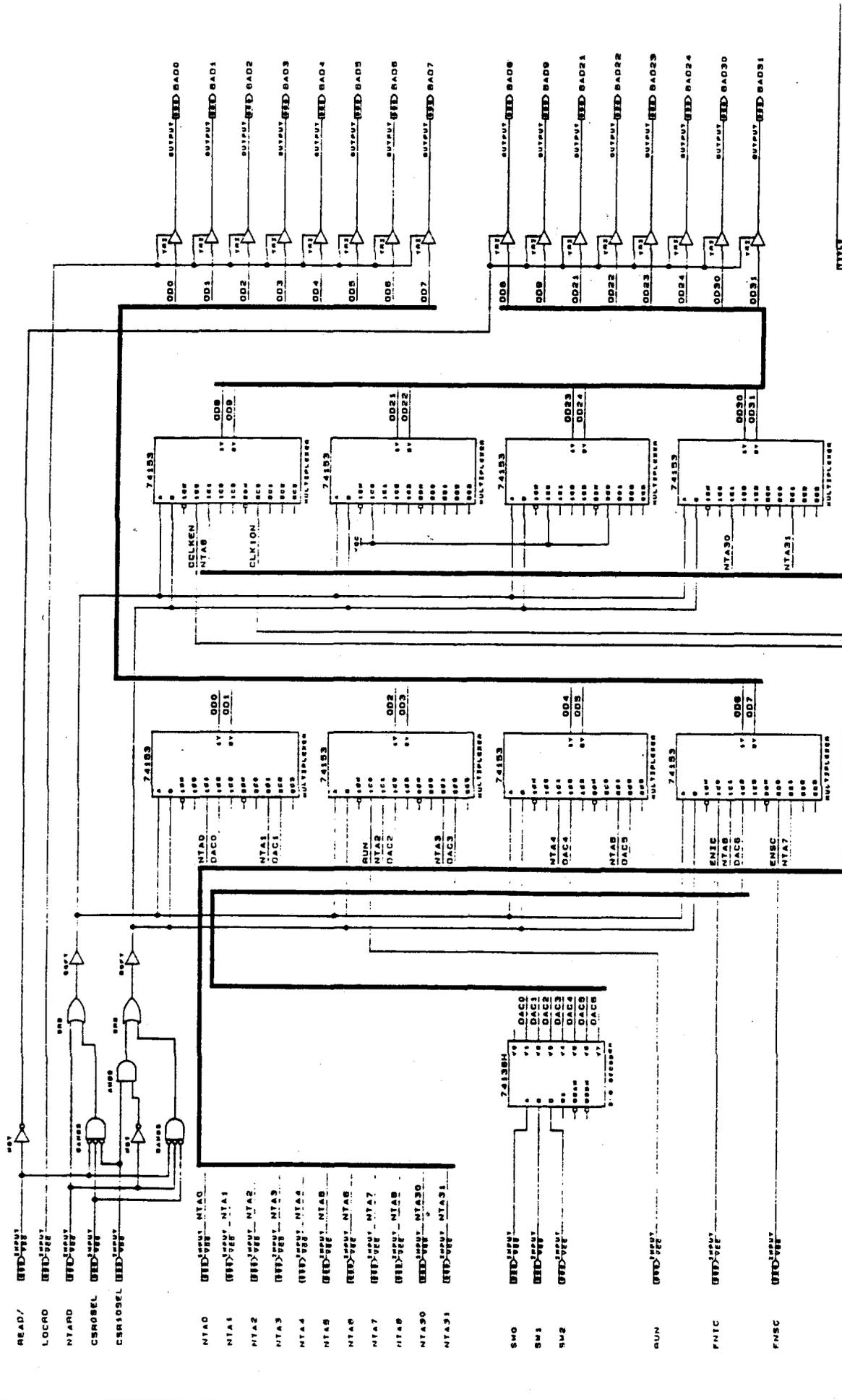
TYPE PA/CMP FASTBUS INTERFACE
 NUMBER 000000
 NAME KEN TREPTON
 DATE 08/24/88
 TIME 11:00 AM
 FILE 8.088.11-13-1880
 SECURITY OFF
 USER SN



TITLE	PA/CMP FB GA SEL LOGIC
COMPANY	FERMILAB
DESIGNER	KEN TREPTOW
SITE C	EPUS EPM5128
DATE	5/11/90
NUMBER	1.00
REV	B
WORK	9
SECURITY	OFF

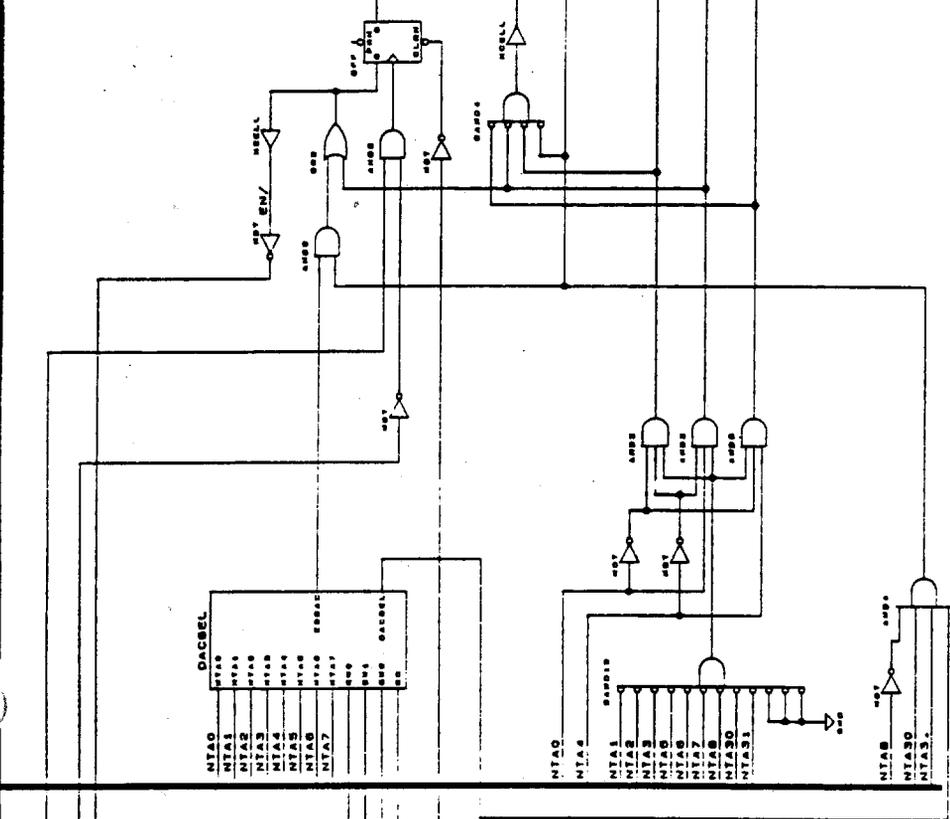


PA/CMF CONTROL LOGIC
 FORM 118B
 KEN TREPTON
 18-188-10-17-1880
 SECURITY

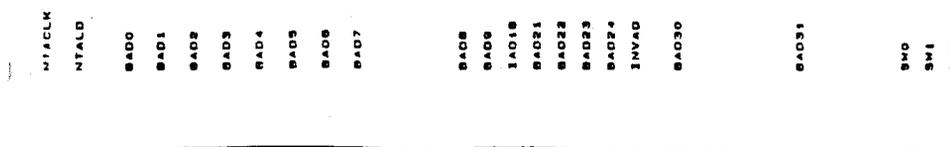


TYPE PA/CMP OUTPUT MUX
 DESIGNED BY Fermilab
 DESIGNED BY KEN TREPTON
 DATE 01/11/82
 DRAWN BY J. G. BERRY
 CHECKED BY J. G. BERRY
 PART NUMBER 18-37-1000
 REV 9

NTA0 D NTA0
 NTA1 INPUT EED NTA1
 NTA2 INPUT EED NTA2
 NTA3 INPUT EED NTA3
 NTA4 OUTPUT EED NTA4
 NTA5 INPUT EED NTA5
 NTA6 OUTPUT EED NTA6
 NTA7 INPUT EED NTA7
 NTA8 OUTPUT EED NTA8
 NTA9 INPUT EED NTA9
 NTA10 INPUT EED NTA10
 NTA11 OUTPUT EED NTA11



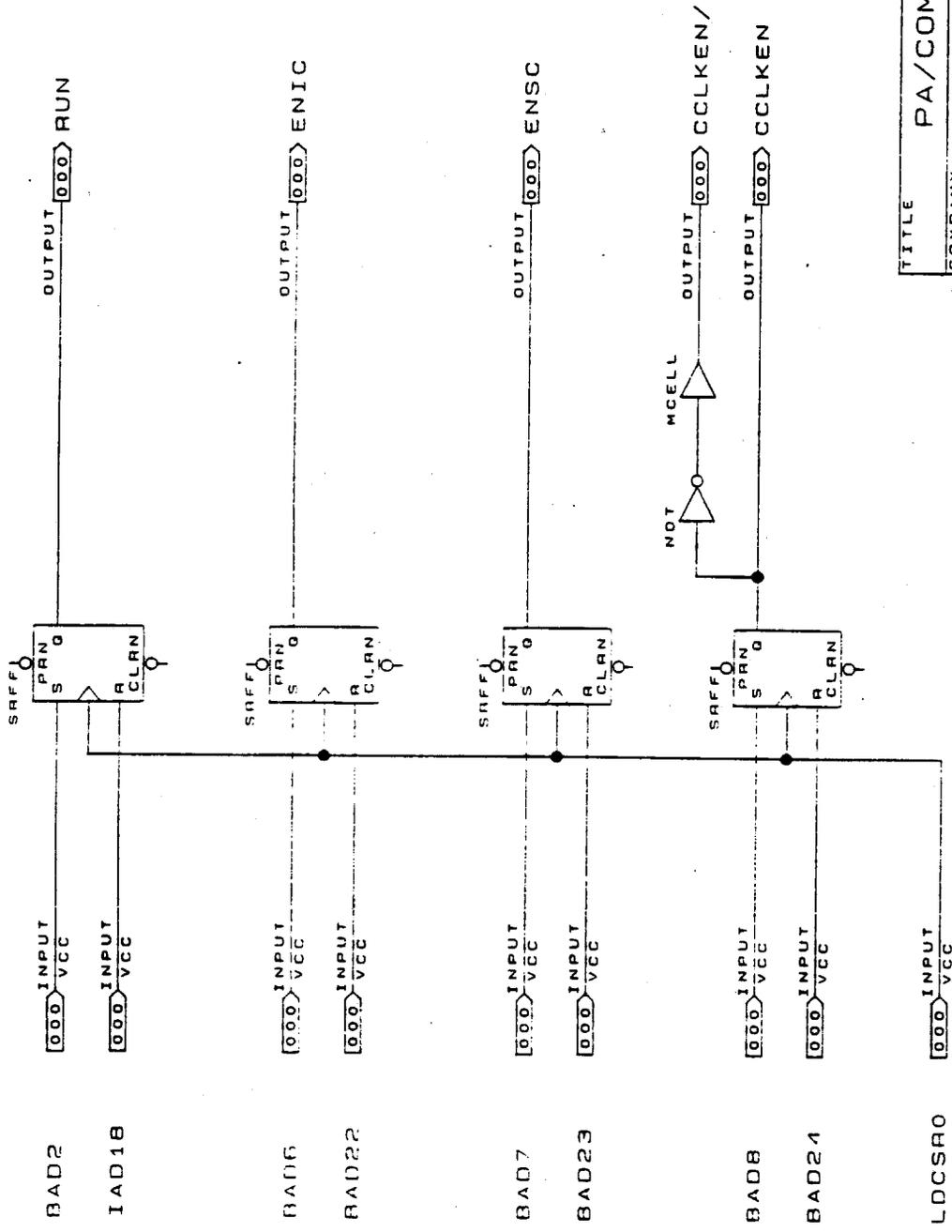
NTA0 DACBEL
 NTA1 DACBEL
 NTA2 DACBEL
 NTA3 DACBEL
 NTA4 DACBEL
 NTA5 DACBEL
 NTA6 DACBEL
 NTA7 DACBEL
 NTA8 DACBEL
 NTA9 DACBEL
 NTA10 DACBEL
 NTA11 DACBEL



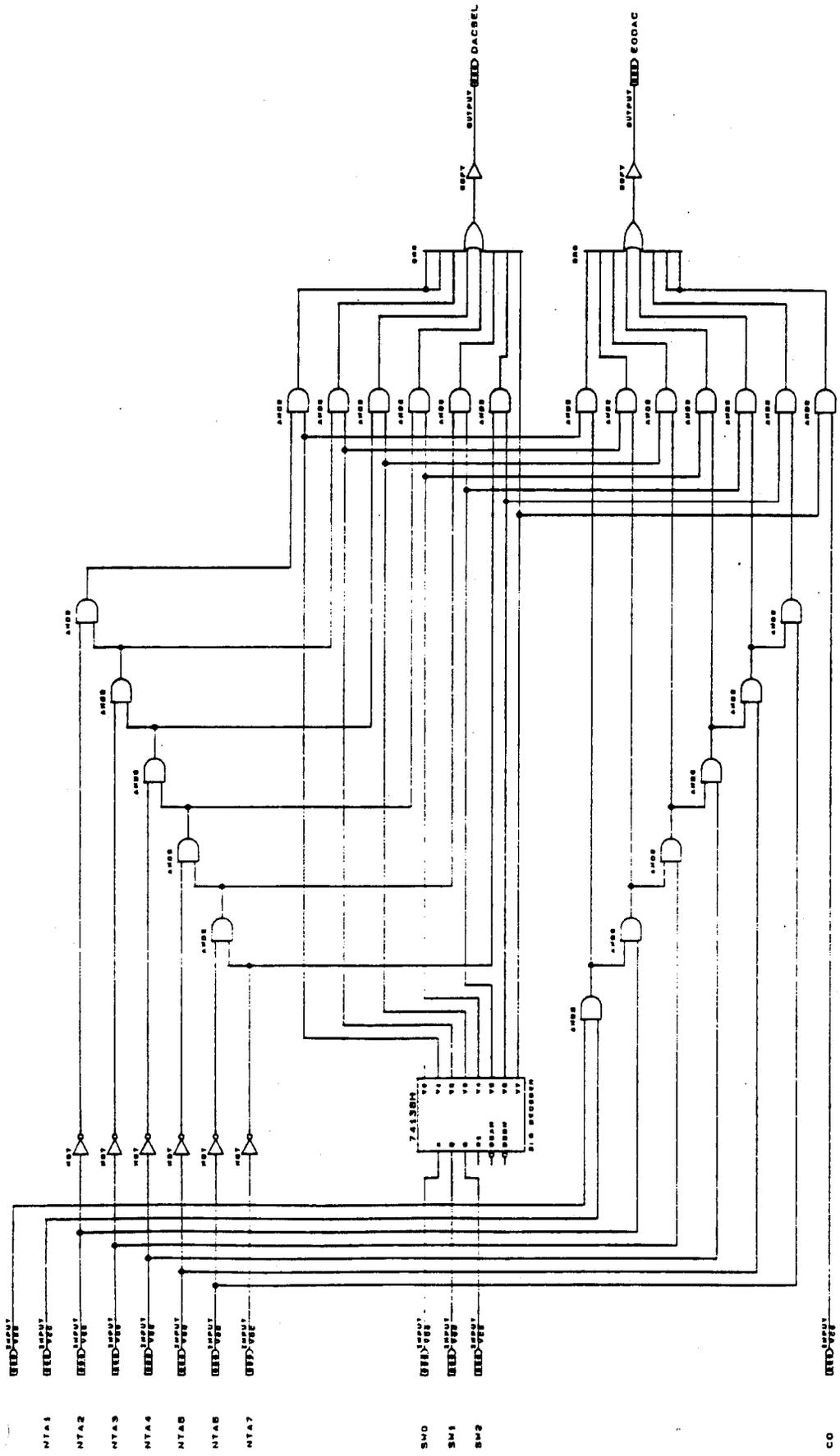
PA/CMP NTA REGISTER
 FORM 1180
 KEN TREPTOW
 10-17-1960
 OFF

NTA0 DACBEL
 NTA1 DACBEL
 NTA2 DACBEL
 NTA3 DACBEL
 NTA4 DACBEL
 NTA5 DACBEL
 NTA6 DACBEL
 NTA7 DACBEL
 NTA8 DACBEL
 NTA9 DACBEL
 NTA10 DACBEL
 NTA11 DACBEL

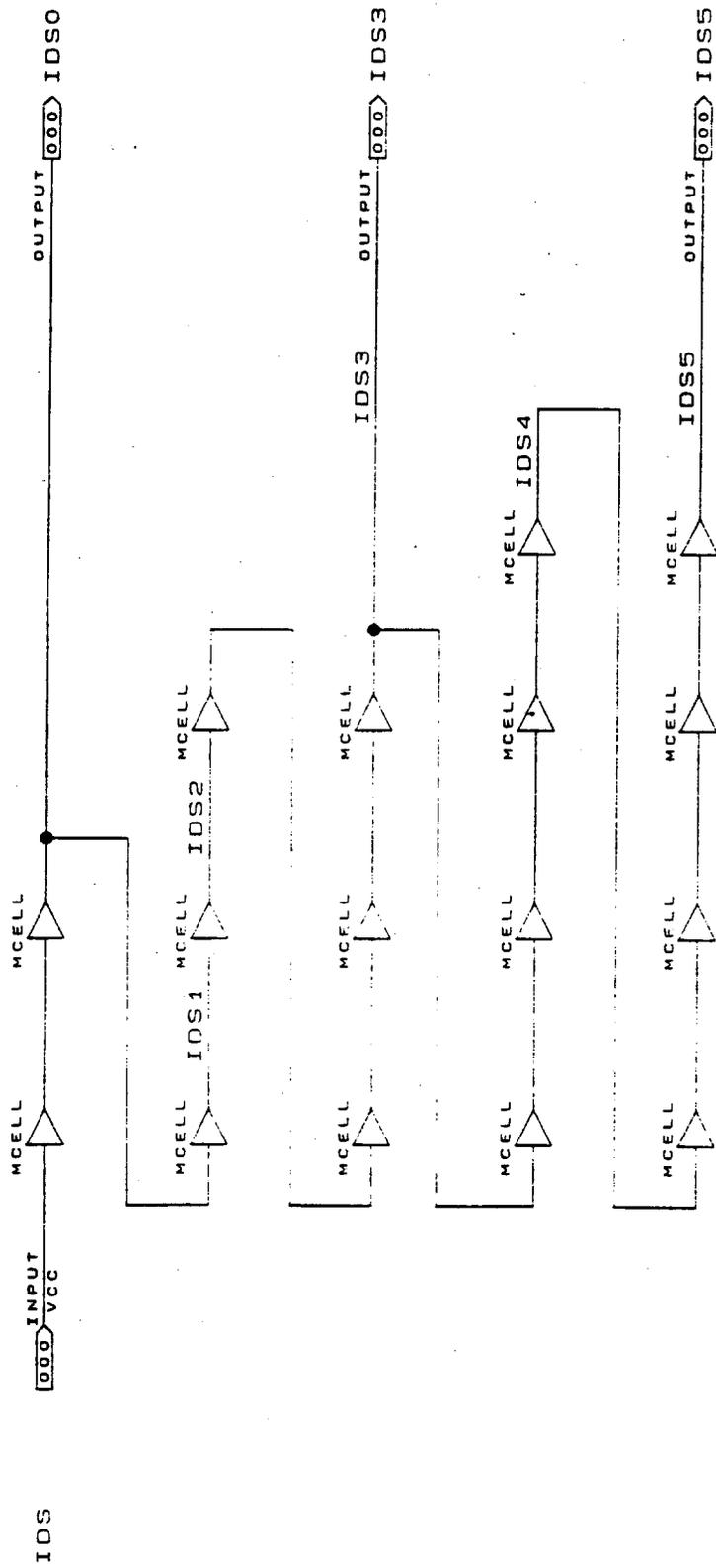




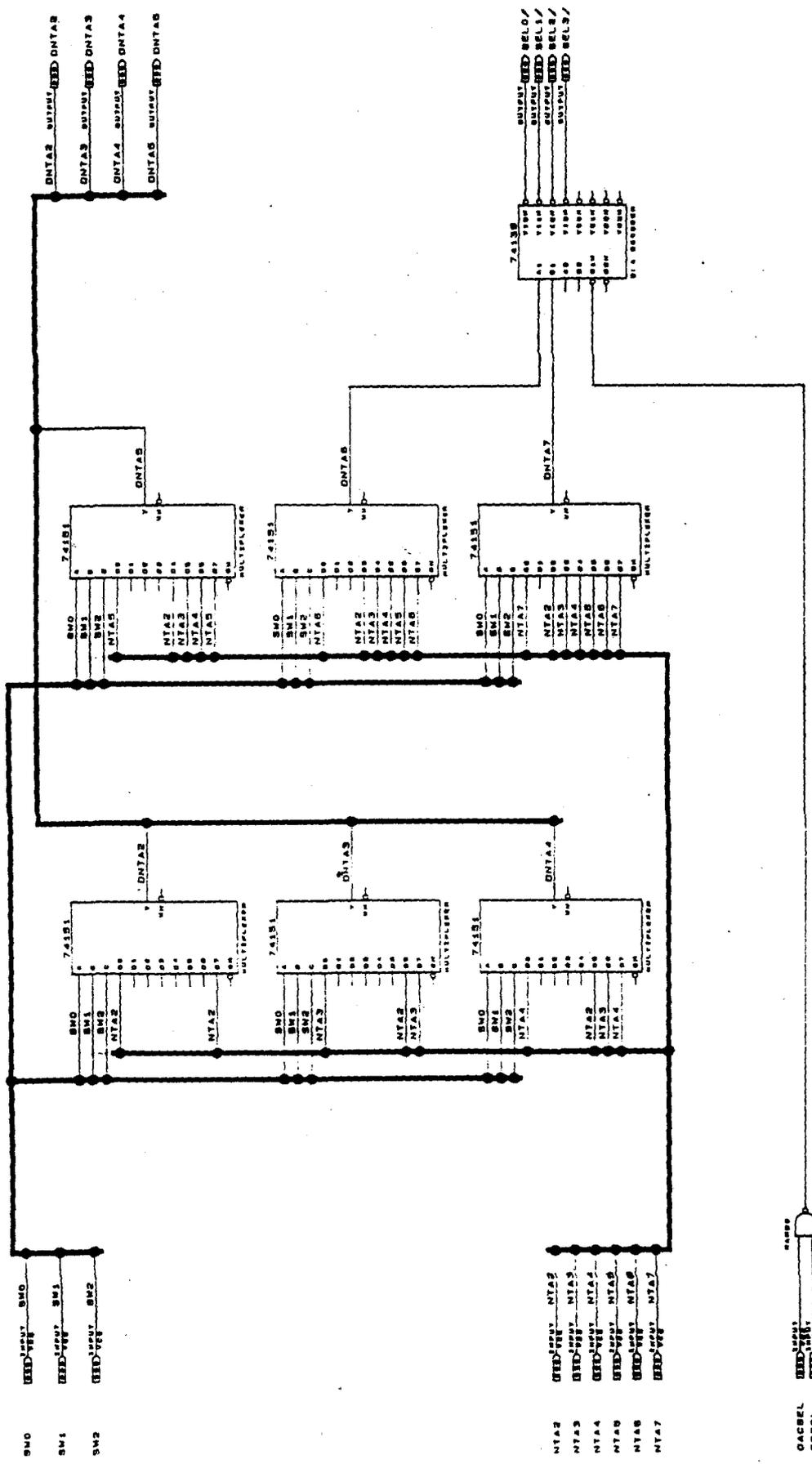
TITLE		PA/COMP CSRO	
COMPANY		FERMILAB/CD/DAE	
DESIGNER		KEN TREPTOW	
SIZE	EPLO	NUMBER	1.00
DATE	6/26/90	SHEET	6 OF 9
TURBO	ON	SECURITY	OFF



TITLE PA/CMP DAC ADDR DECODE
 DESIGN F87M180
 DESIGNER KEN TREPTON
 DATE 11/13/88
 DRAWN 1-08
 CHECKED 11/13/88
 SECURITY OFF

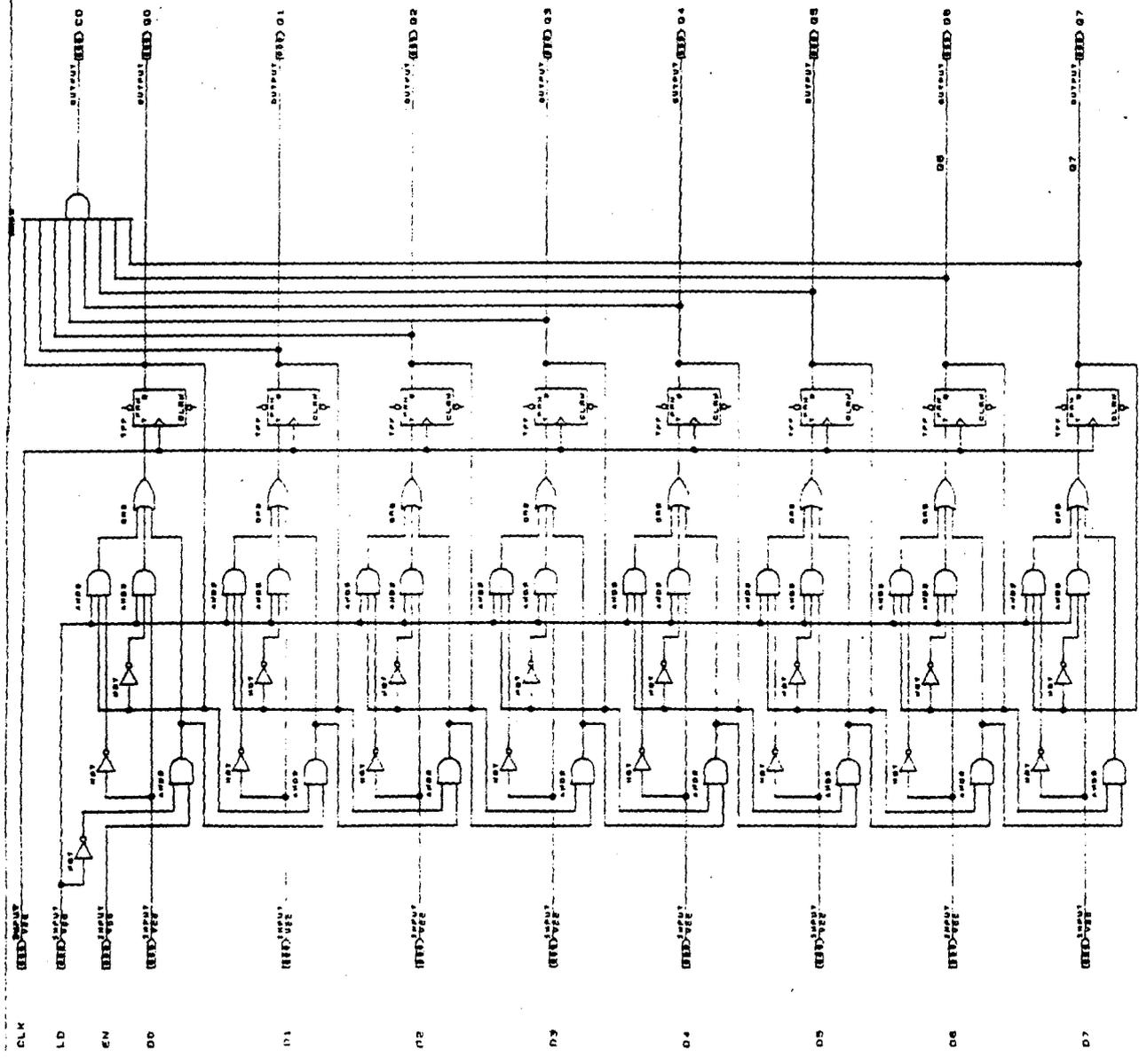


TITLE	PA/CMP DS DELAYS		
COMPANY	Fermilab		
DESIGNER	KEN TREPTOW		
SIZE	8	EPLD	EP5128
DATE	10:22a 11-13-1990		NUMBER 1.00 REV A
TURBO	ON	SECURITY	OFF



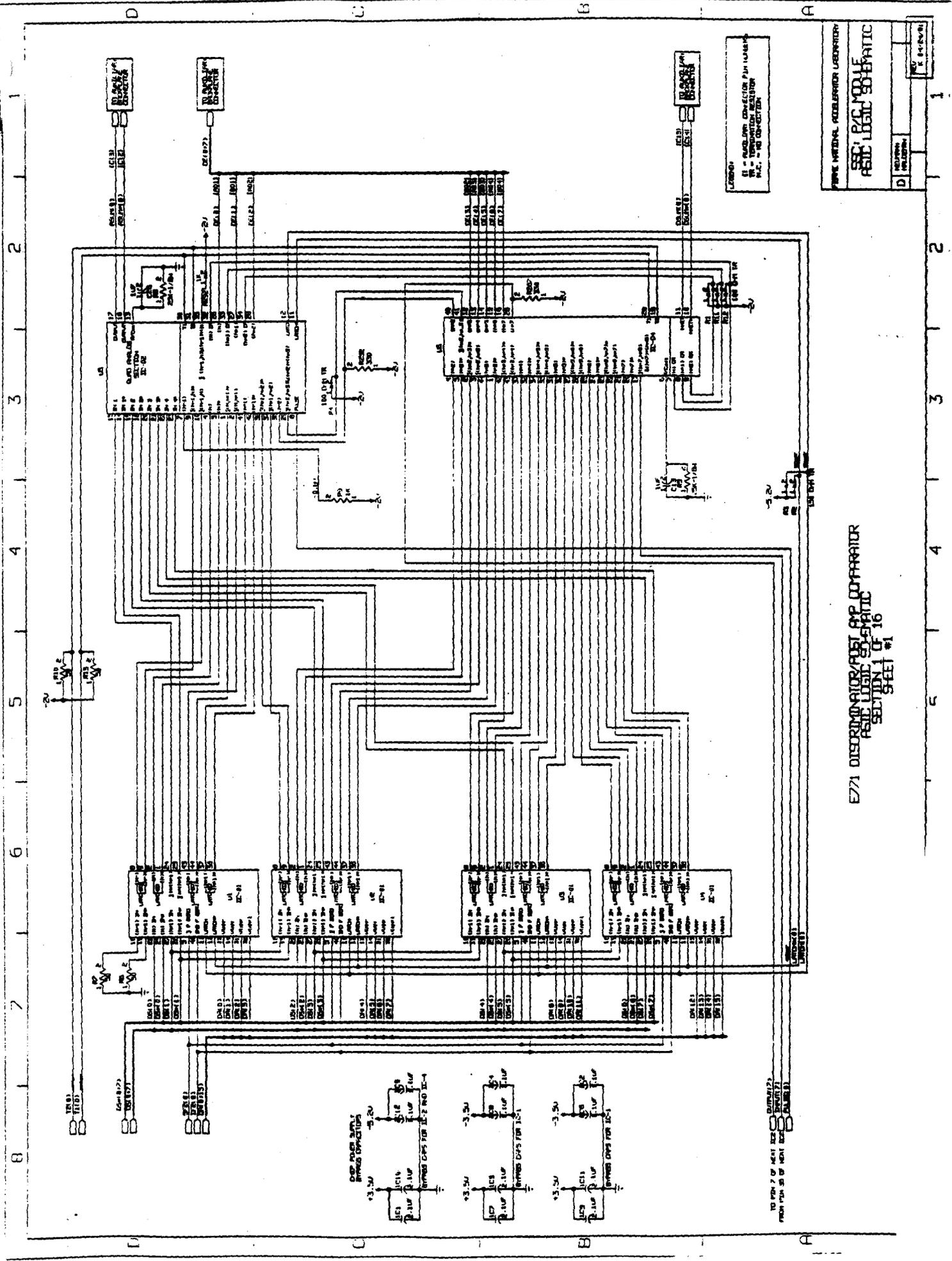
TYPE PA/CMP DAC MAPPING LOGI
 NUMBER F8M118B/CO/DAE
 SYSTEM KEN TREPION
 DATE 10 DEC 1980
 TIME 10:00
 USER P. HARRIS
 JOB P. HARRIS
 UNIT 11-18-1880 SECURITY OFF
 ON

GACBEL
 FBSEL
 11-18-1880



TITLE 8-BIT COUNTER
 NUMBER FERMILAB/RD/EEO/DES
 DESIGNER KEN TREPTON
 DATE 10/19/68
 REVISION 1
 NUMBER 1-90
 MODEL 8/8/68
 PROJECT 01
 DRAWN BY

APPENDIX C - POSTAMP/COMPARATOR MODULE - SCHEMATIC

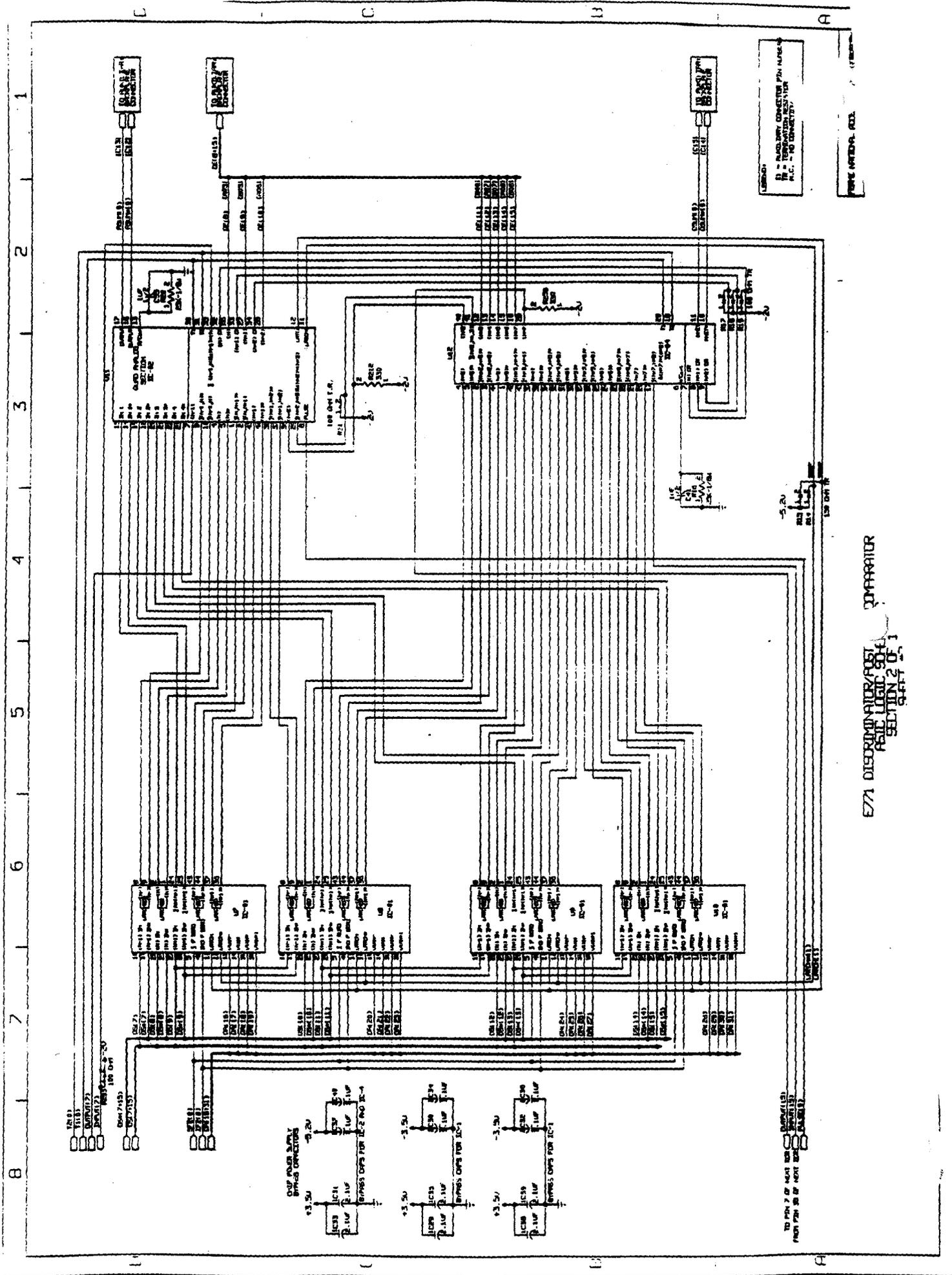


E771 DISCRIMINATOR/PULSAR APD COMPARATOR
 ASIC LOGIC SCHEMATIC
 SECTION 1 OF 16
 SHEET #1

TRIPLE WIRELINE CONNECTION LABORATORY
 5500 PLYMOUTH ROAD
 FORT BELLEVILLE, ILLINOIS 62239
 D. H. HARRIS
 10/1/71

LEGEND:
 (1) - PIANO WIRE CONNECTION PIN 14/14A/B
 (2) - TERMINATION RESISTOR
 (3) - NO DISPOSITION

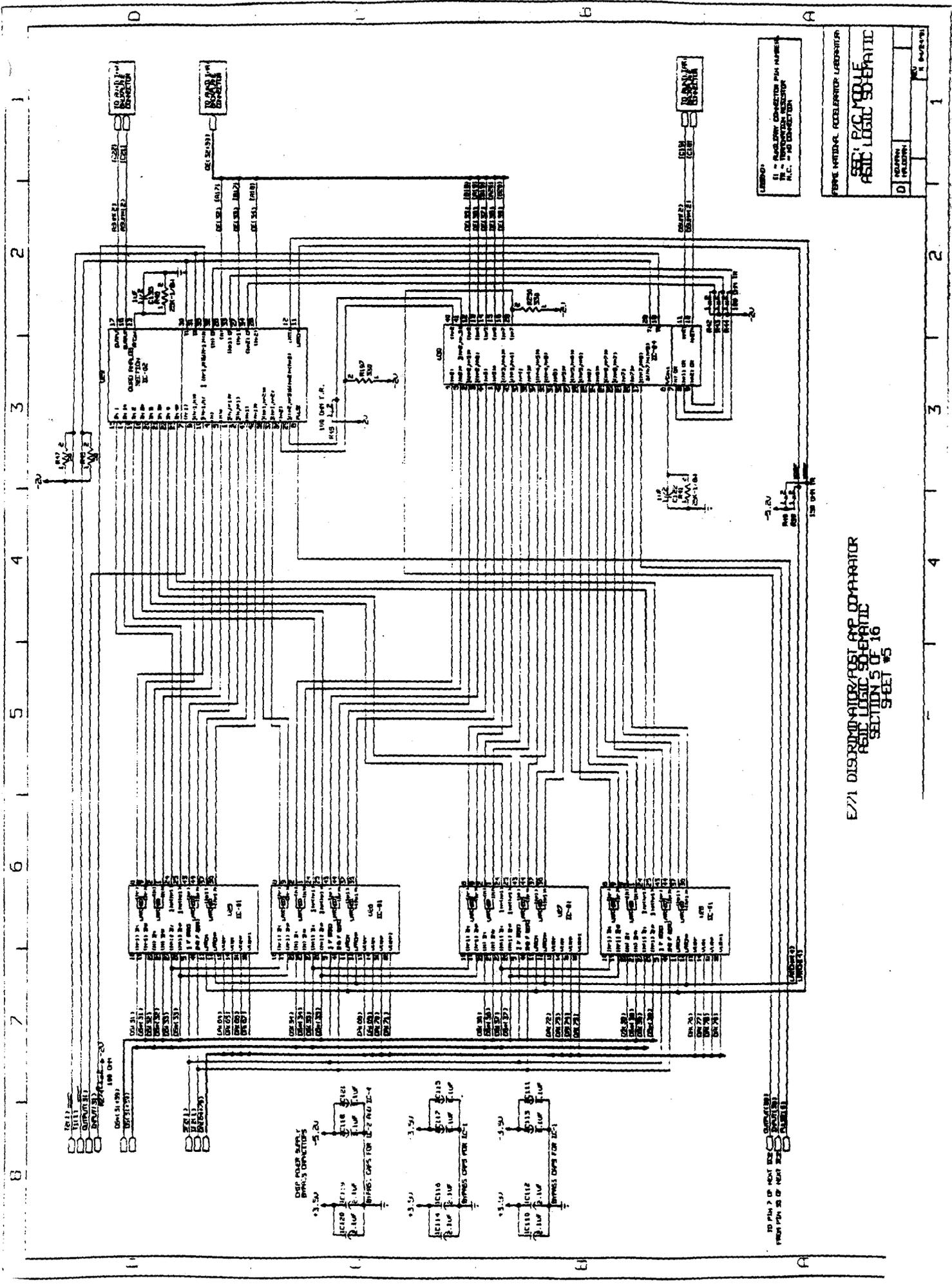
TO PIN 7 OF HEAT SINK (DRAINAGE)
 FROM PIN 25 OF HEAT SINK (GROUND)



E771 DISCRIMINATOR/POST
ASIC LOGIC 90-44
SECTION 2 OF 1

APPENDIX D - MODULE DRAWINGS

1.	2563.000-ED-215747	EED E771 - POST AMP COMPARATOR VER III SCHEMATIC DIAGRAM	REV. I
2.	2563.000-MD-215752	EED E771 - POST AMP COMPARATOR VER III FRONT PANEL & FRONT PANEL AIR GAP FILLER DETAILS	REV. A
3.	2563.000-MD-215753	EED E771 - POST AMP COMPARATOR VER III FRONT PANEL SILK-SCREEN	REV. C
4.	2563.000-MD-215790	EED E771 - POST AMP COMPARATOR VER III DRILL DRAWING	REV. -
5.	2563.000-MD-215802	EED E771 - POST AMP COMPARATOR VER III BOARD LAYUP AND OUTLINE DETAILS	REV. -
6.	2563.000-MD-215803	EED E771 - POST AMP COMPARATOR VER III P.C. BOARD ASSEMBLY	REV. -
7.	2563.000-MD-215804	EED E771 - POST AMP COMPARATOR VER III BOTTOM SIDE ASSEMBLY	REV. -
8.	2563.000-MD-215805	EED E771 - POST AMP COMPARATOR VER III TOP ASSEMBLY	REV. A
9.	2563.000-MD-215806	EED E771 - POST AMP COMPARATOR VER III LED AND TEST POINTS WIRING DETAILS	REV. -
10.	2563.000-MD-215807	EED E771 - POST AMP COMPARATOR VER III DAC JUMPER DIAGRAM	REV. -
11.	2563.000-MD-215808	EED E771 - POST AMP COMPARATOR VER III POWER TEST POINTS DETAILS	REV. -

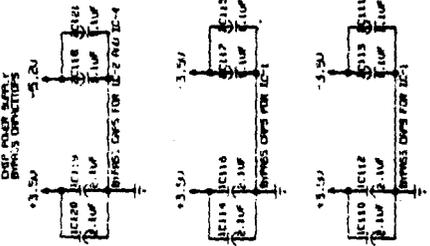


E771 DISBURSMENT/POST FIRE COMPARTOR
 ASIC LOGIC SCHEMATIC
 SECTION 5 OF 16
 SHEET #5

LEGEND:
 II - PACKAGING CONNECTOR PINS NUMBER
 IN - INPUT SIGNAL
 ALL - NO CONNECTION

SERIES MATERIAL ACCELERATOR LABORATORY	
ASIC LOGIC SCHEMATIC	
D	REVISION
	DATE

TO PIN 3 OF NEXT IC OR
 FROM PIN 2 OF NEXT IC
 ALL OTHERS



1 2 3 4 5 6 7 8

1 2 3 4

D

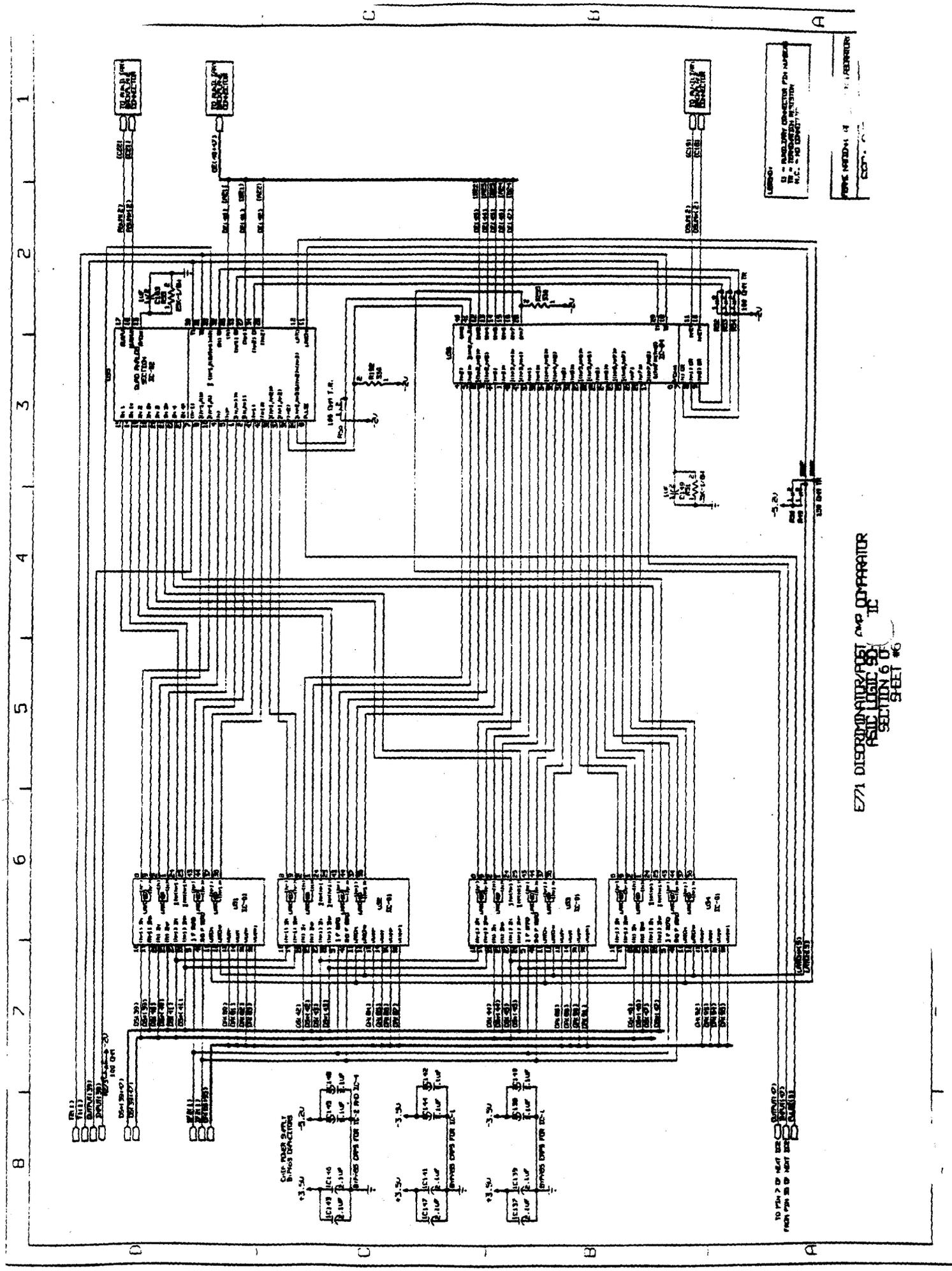
B

A

E

C

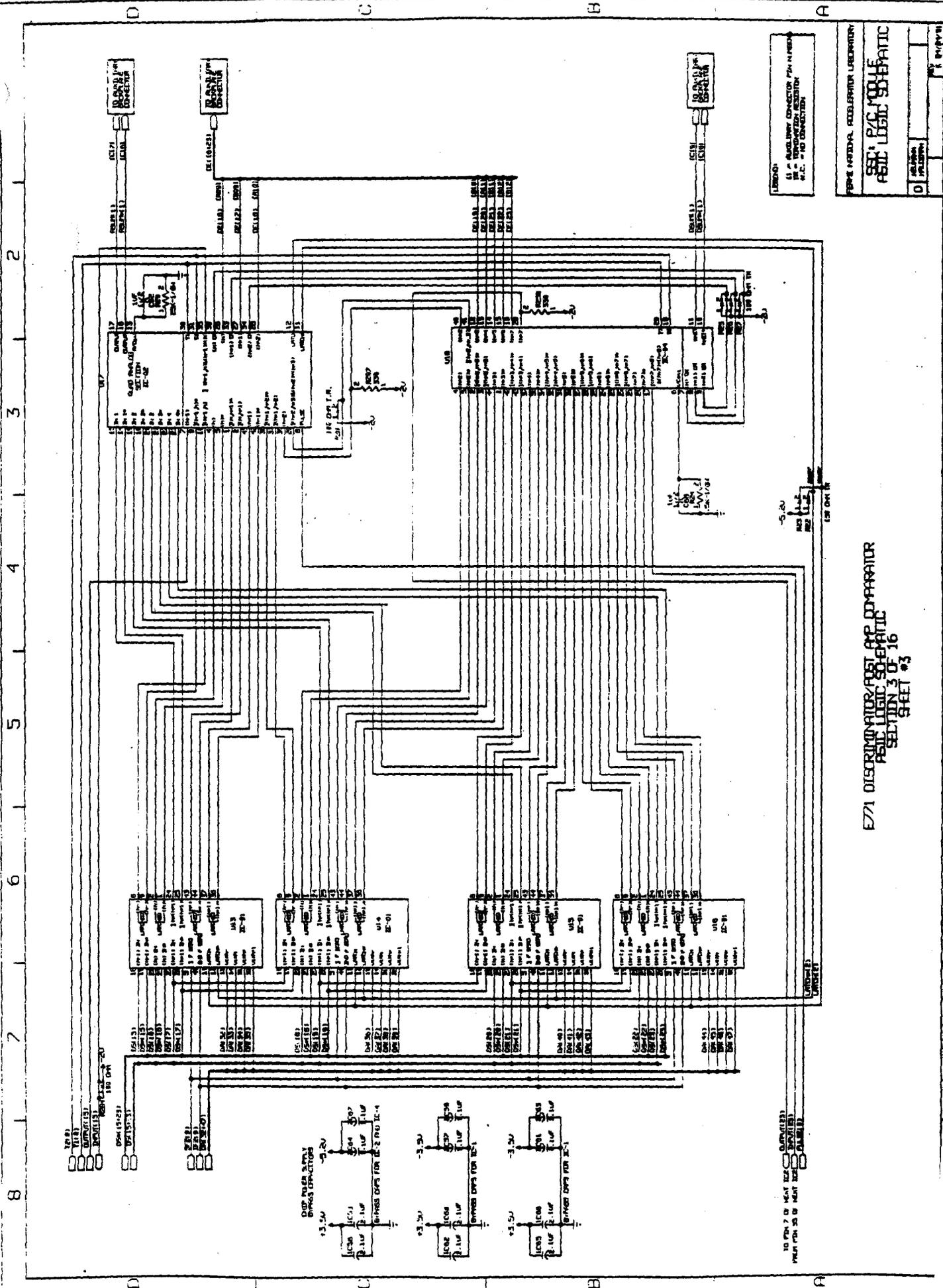
A



E771 DISCRIMINATOR/SET AND COMPARATOR
 ASIC LOGIC 50
 SECTION 6 OF
 SHEET #6

UNLESS OTHERWISE SPECIFIED
 ALL DIMENSIONS ARE IN MILLIMETERS
 UNLESS OTHERWISE SPECIFIED

TO PIN 2 OF 7414, 7415, 7416, 7417, 7418, 7419, 7420, 7421, 7422, 7423, 7424, 7425, 7426, 7427, 7428, 7429, 7430, 7431, 7432, 7433, 7434, 7435, 7436, 7437, 7438, 7439, 7440, 7441, 7442, 7443, 7444, 7445, 7446, 7447, 7448, 7449, 7450, 7451, 7452, 7453, 7454, 7455, 7456, 7457, 7458, 7459, 7460, 7461, 7462, 7463, 7464, 7465, 7466, 7467, 7468, 7469, 7470, 7471, 7472, 7473, 7474, 7475, 7476, 7477, 7478, 7479, 7480, 7481, 7482, 7483, 7484, 7485, 7486, 7487, 7488, 7489, 7490, 7491, 7492, 7493, 7494, 7495, 7496, 7497, 7498, 7499

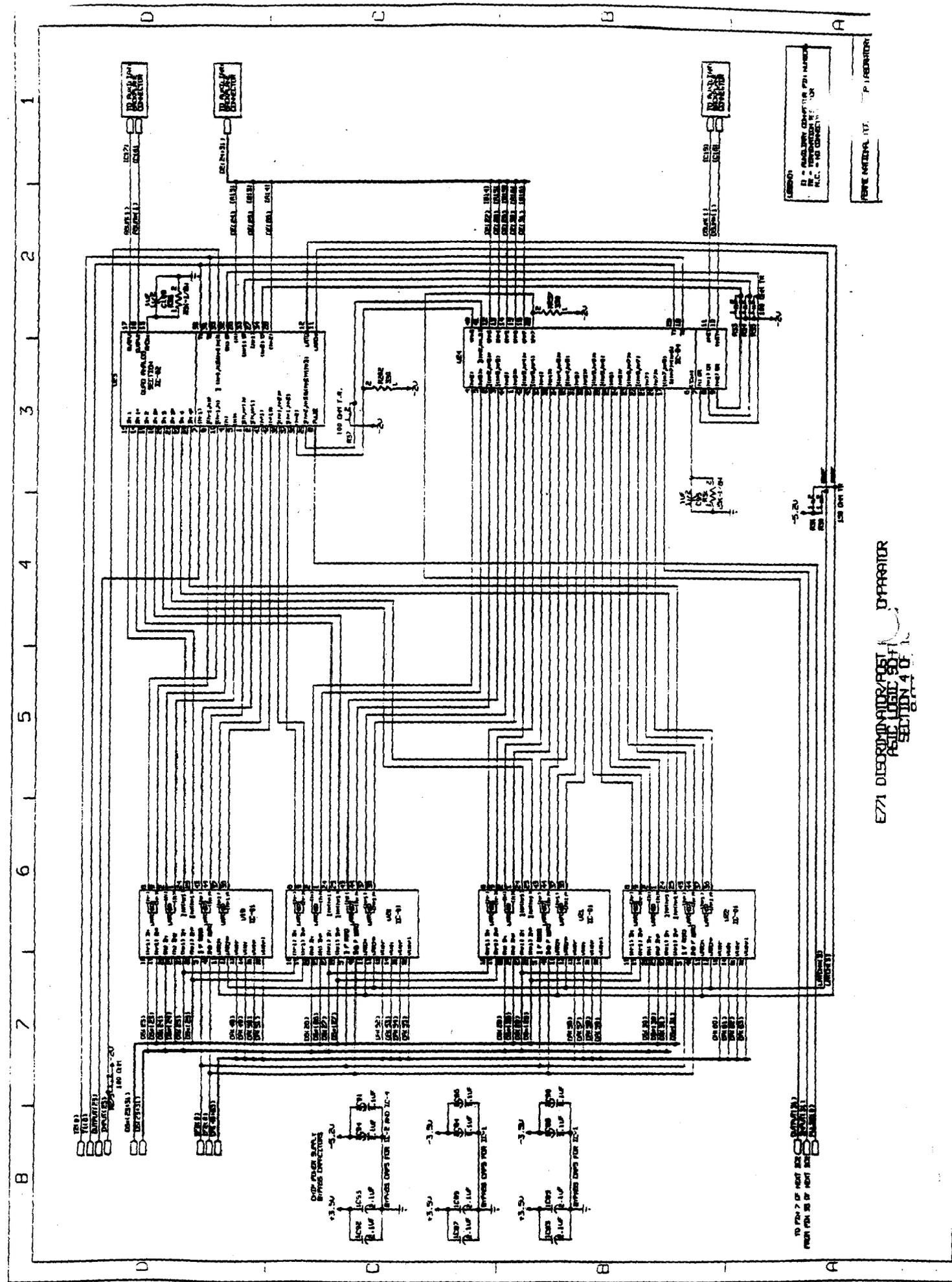


E71 DISCRIMINATOR/FAST AMP COMPARATOR
 BASIC LOGIC SCHEMATIC
 SECTION 3 OF 16
 SHEET #3

UNLESS OTHERWISE SPECIFIED
 ALL DIMENSIONS ARE IN INCHES
 UNLESS OTHERWISE SPECIFIED
 ALL DIMENSIONS ARE IN MILLIMETERS

FORMERLY RESEARCH LABORATORY
 SRI: PACIFIC SOUTHERN
 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100

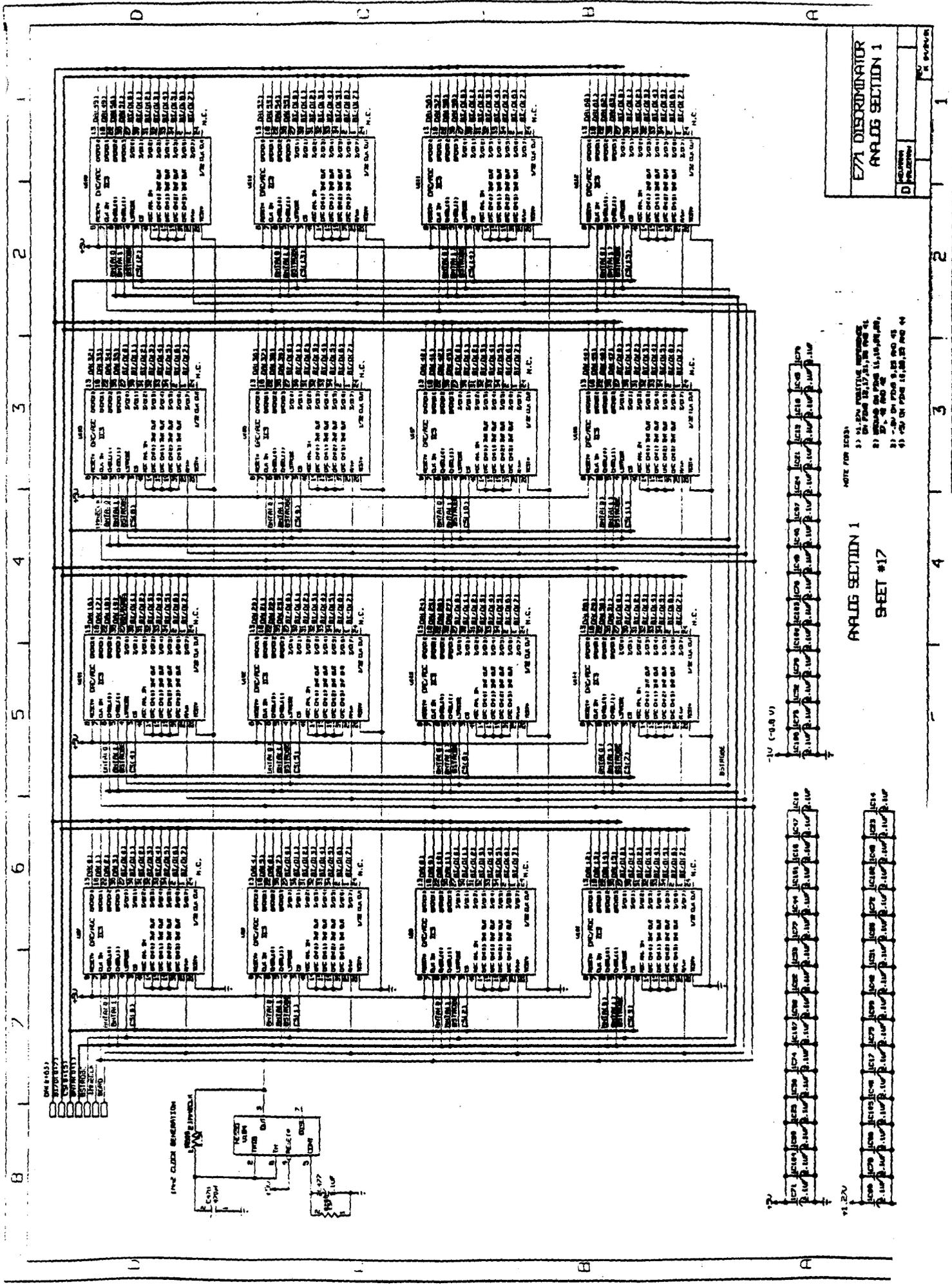
10 PIN 7 OF MNT 122
 10 PIN 25 OF MNT 122
 10 PIN 1 OF MNT 122



E71 DISCRIMINATOR/POST AMPLIFIER LOGIC SECTION 40

0222 0223 0224
 BLACK BOX CONNECTOR
 P. 1. IDENTIFICATION

TO PIN 7 OF PORT 202 (0201)
 FROM PIN 30 OF PORT 202 (0201)



E7A DISCRIMINATOR
ANALOG SECTION 1

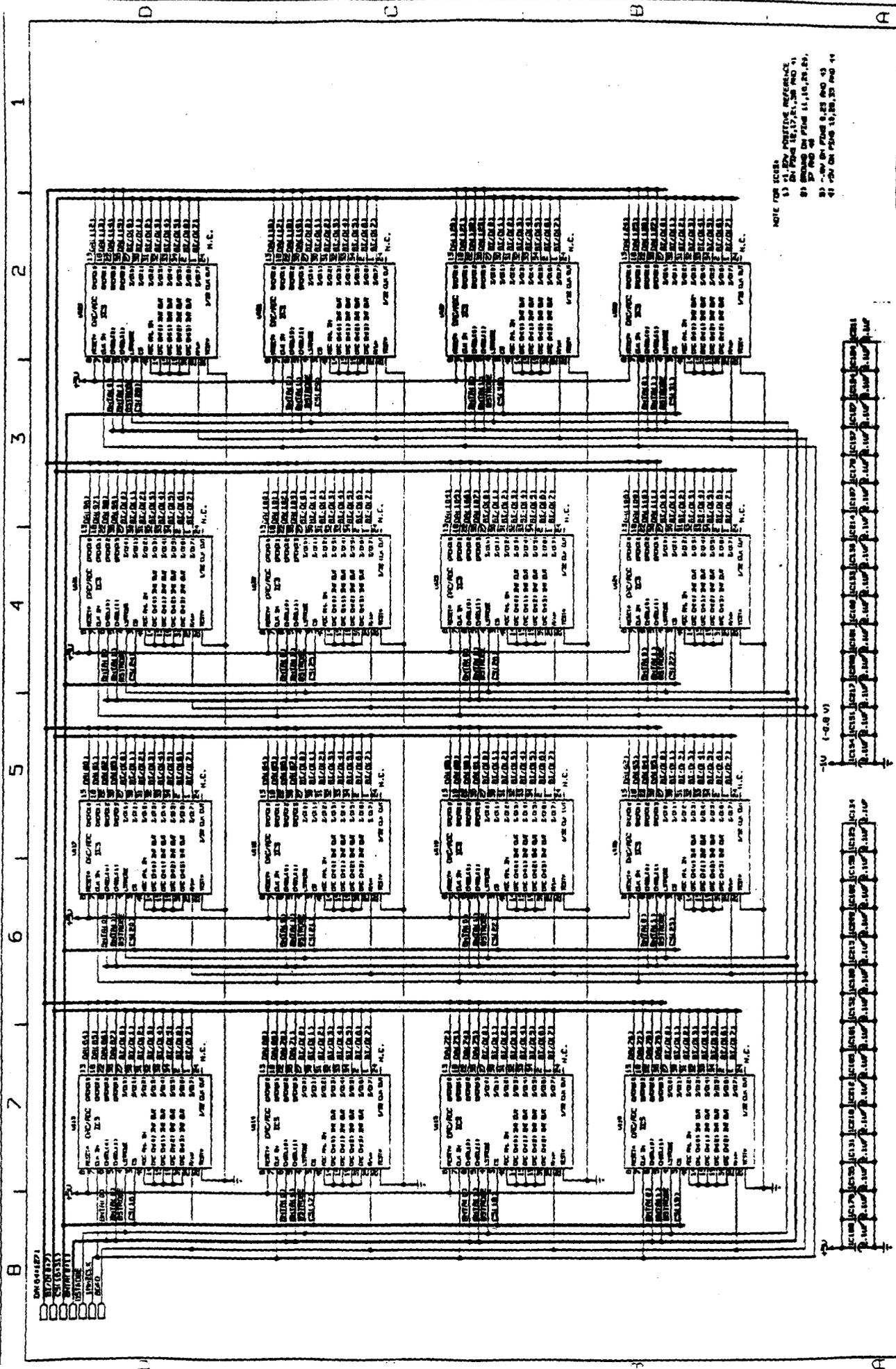
REV	DESCRIPTION
1	AS SHOWN

NOTE FOR ISSUES
 1) 14.024 POSITIVE REFERENCE ON PAGES 12, 17, 21, 26, 28, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100

ANALOG SECTION 1
 SHEET #17

14 (9.8 V)

11.2V



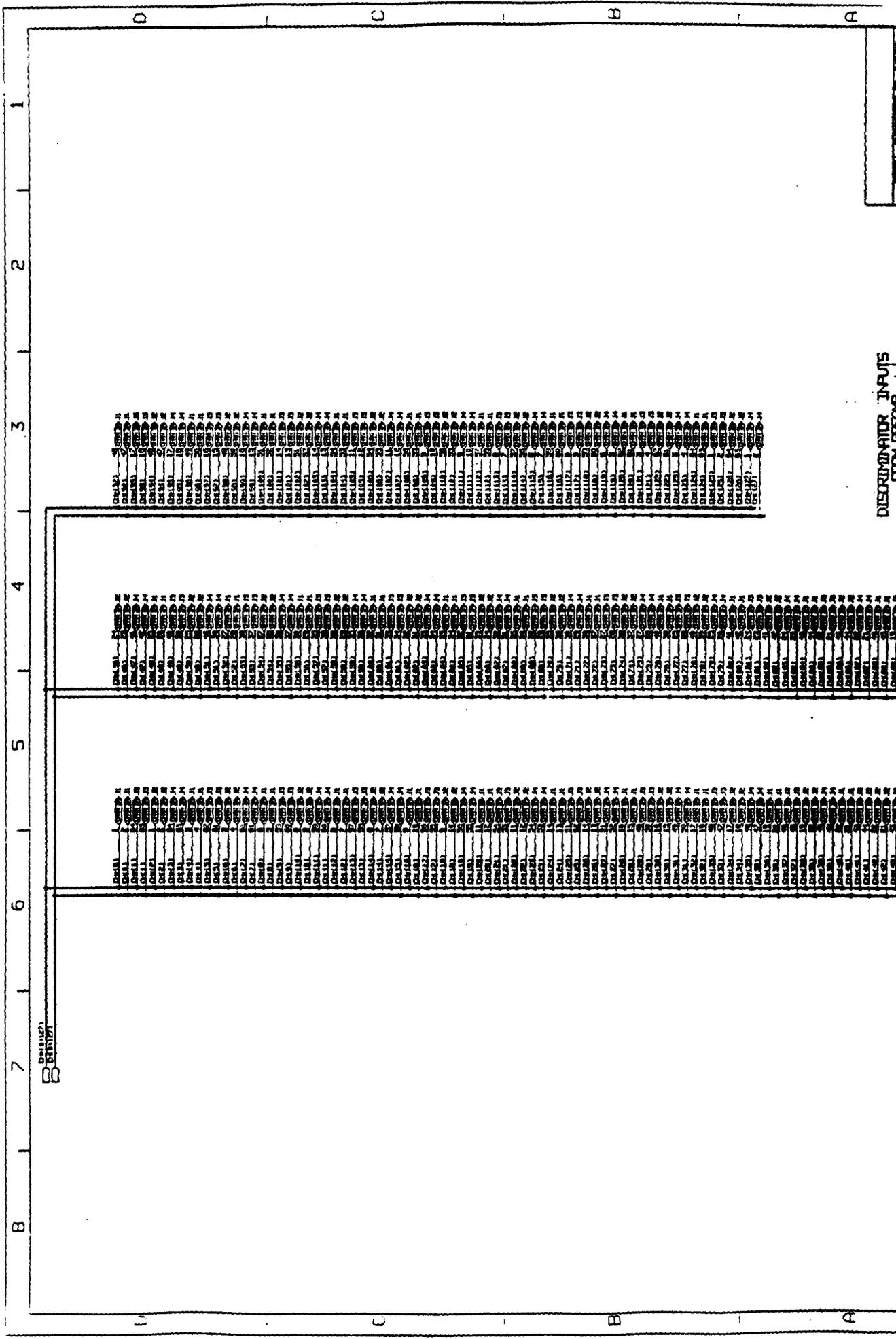
NOTE FOR SCHEMATIC
 1) 100% POSITIVE REFERENCE
 2) 100% POSITIVE REFERENCE
 3) 100% POSITIVE REFERENCE
 4) 100% POSITIVE REFERENCE

ANALOG SECTION 2

10 (4-8-0)

081041E21

41 20



E71 DISCRIMINATOR INPUS
 DISCRIMINATOR INPUS
 FROM FREAMP

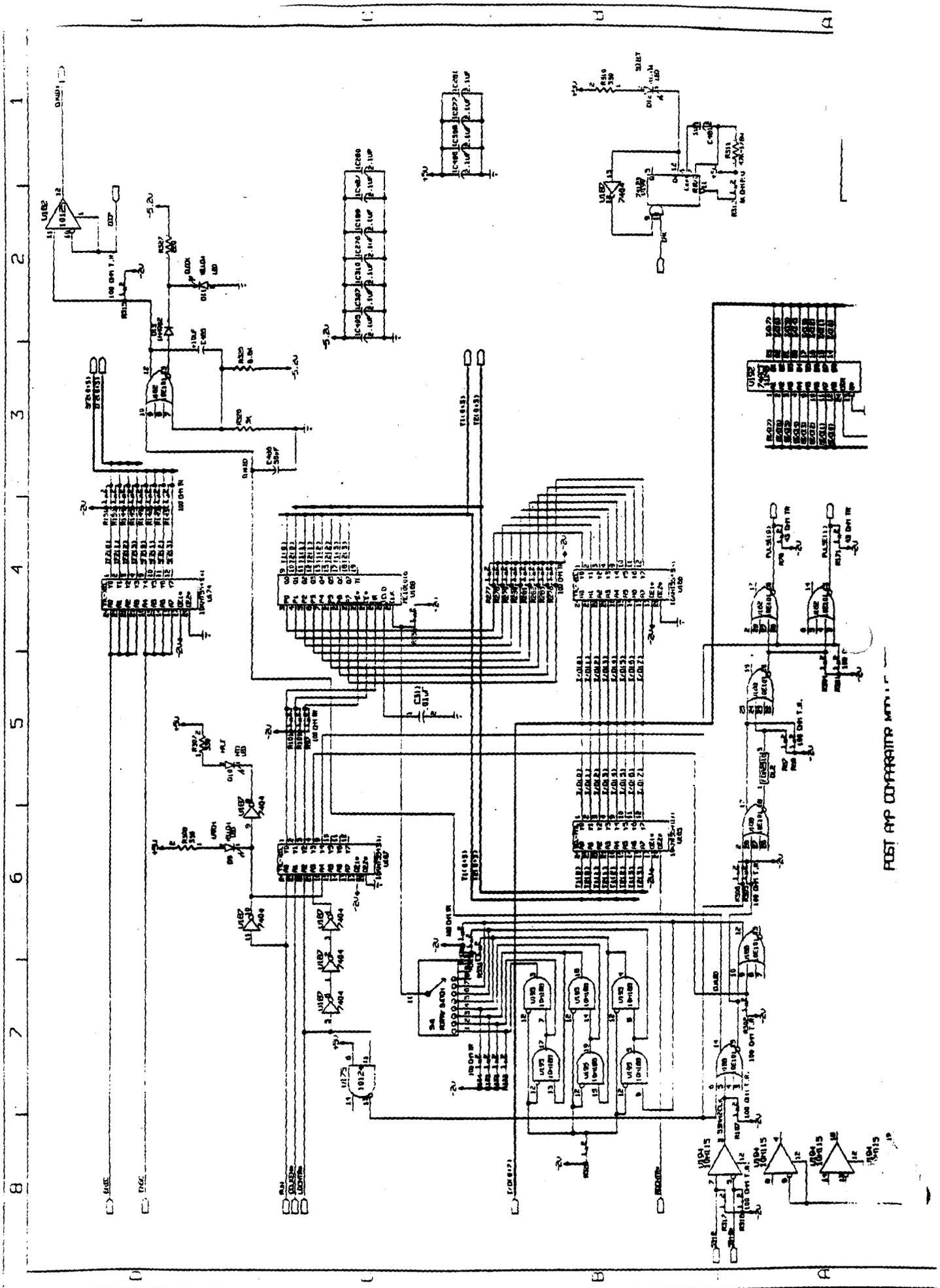
DISCRIMINATOR INPUS
 FROM FREAMP
 SHEET #23

DA11021
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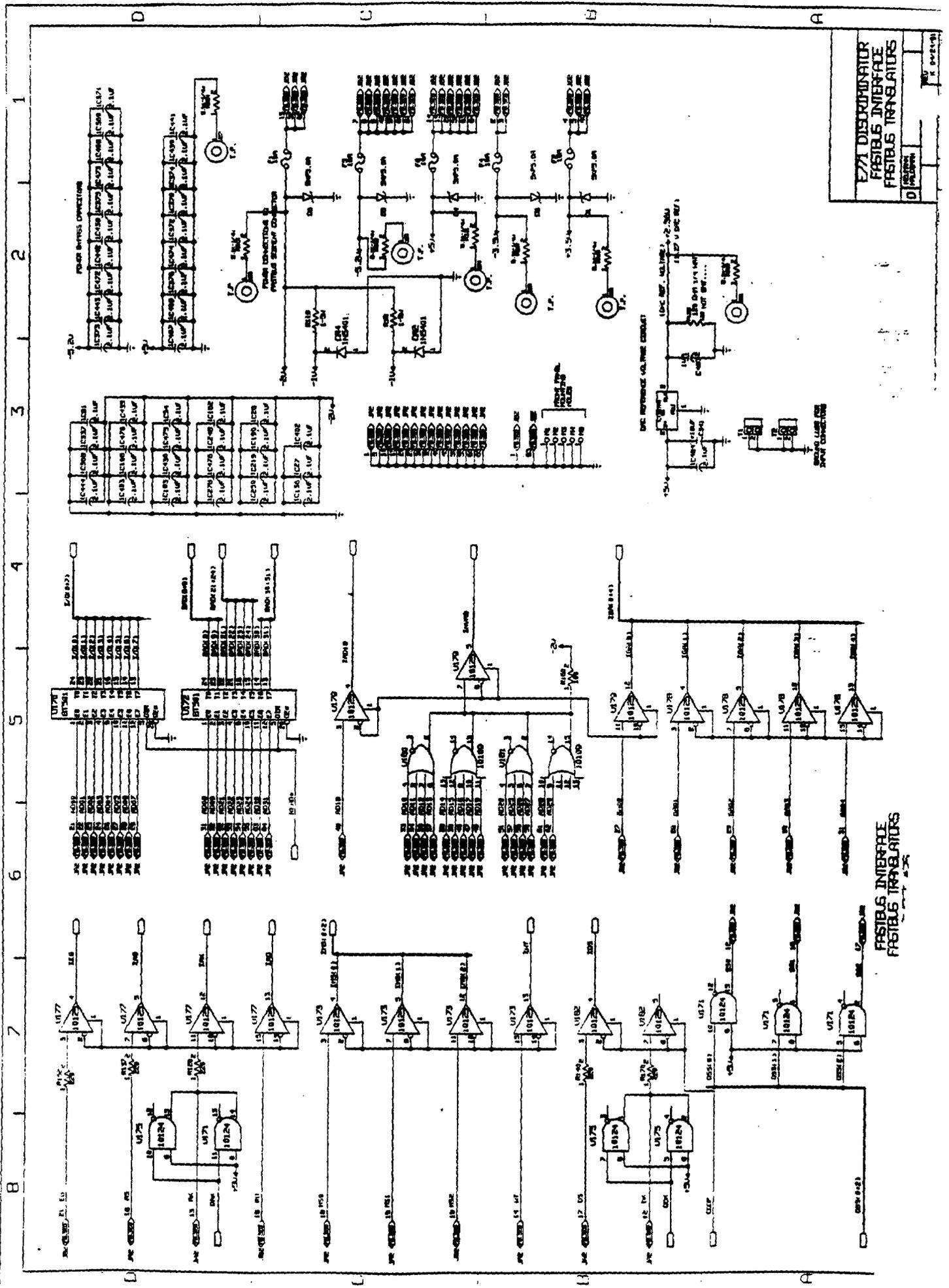
DA11101
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 DA11300

DA11301
 DA11302



POST ARITH COMPARATOR



771 DISCRIMINATOR
FASTBUS INTERFACE
FASTBUS TRANSLATORS

FASTBUS INTERFACE
FASTBUS TRANSLATORS

1 2 3 4 5 6 7 8

D C B A

01

01

01

01

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01

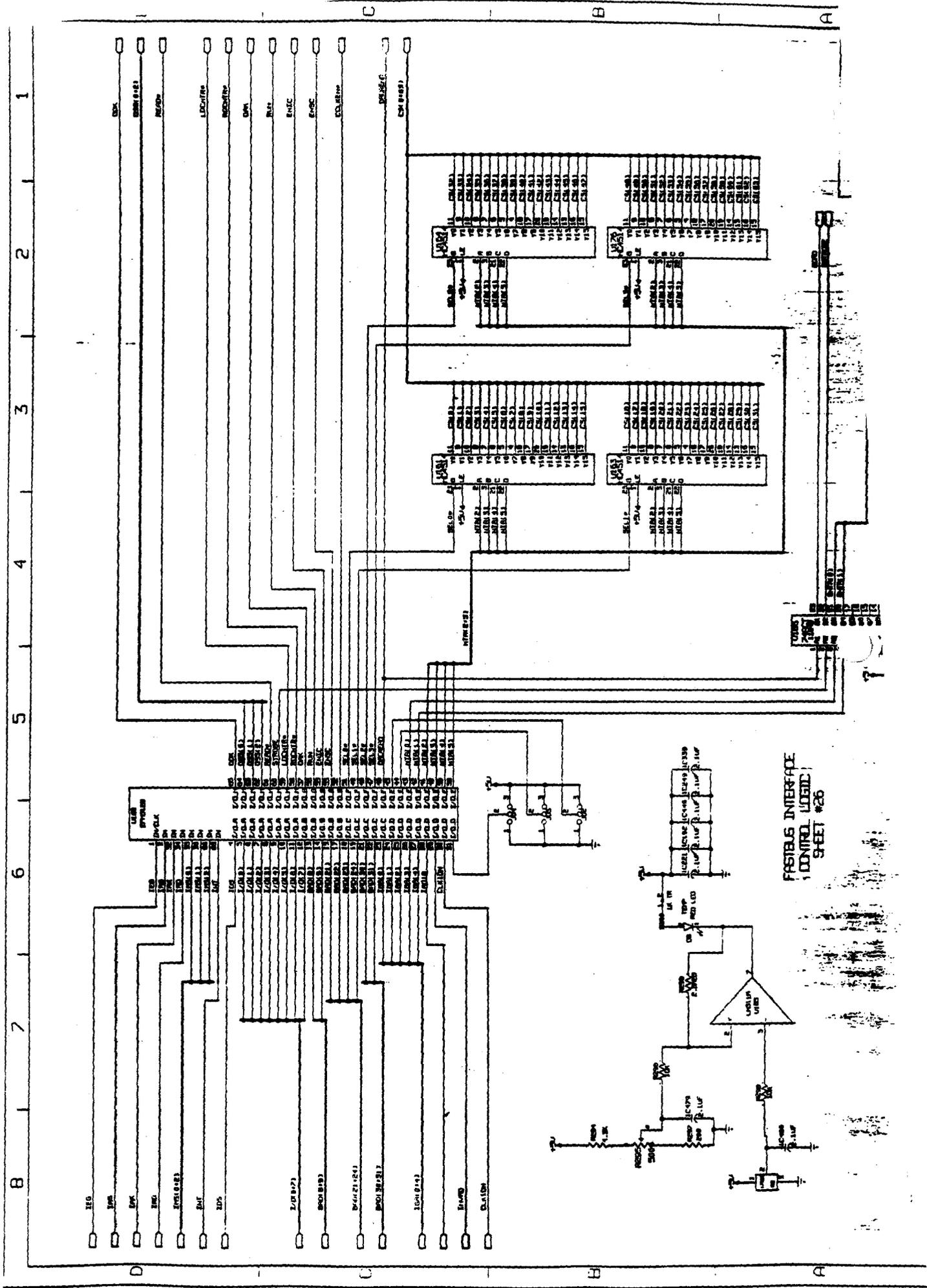
01

01

01

01

01



FASTBUS INTERFACE
CONTROL LOGIC
SHEET #28

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D — C — B — A

OF7
OF8
OF9

FIDUCIALS

OT3
OT4
OT5
OT6

TOOLING HOLES

NECESSARY TO MANUFACTURE
THE PRINTED CIRCUIT BOARD

A

REV K 04/24/91

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D — C — B — A

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

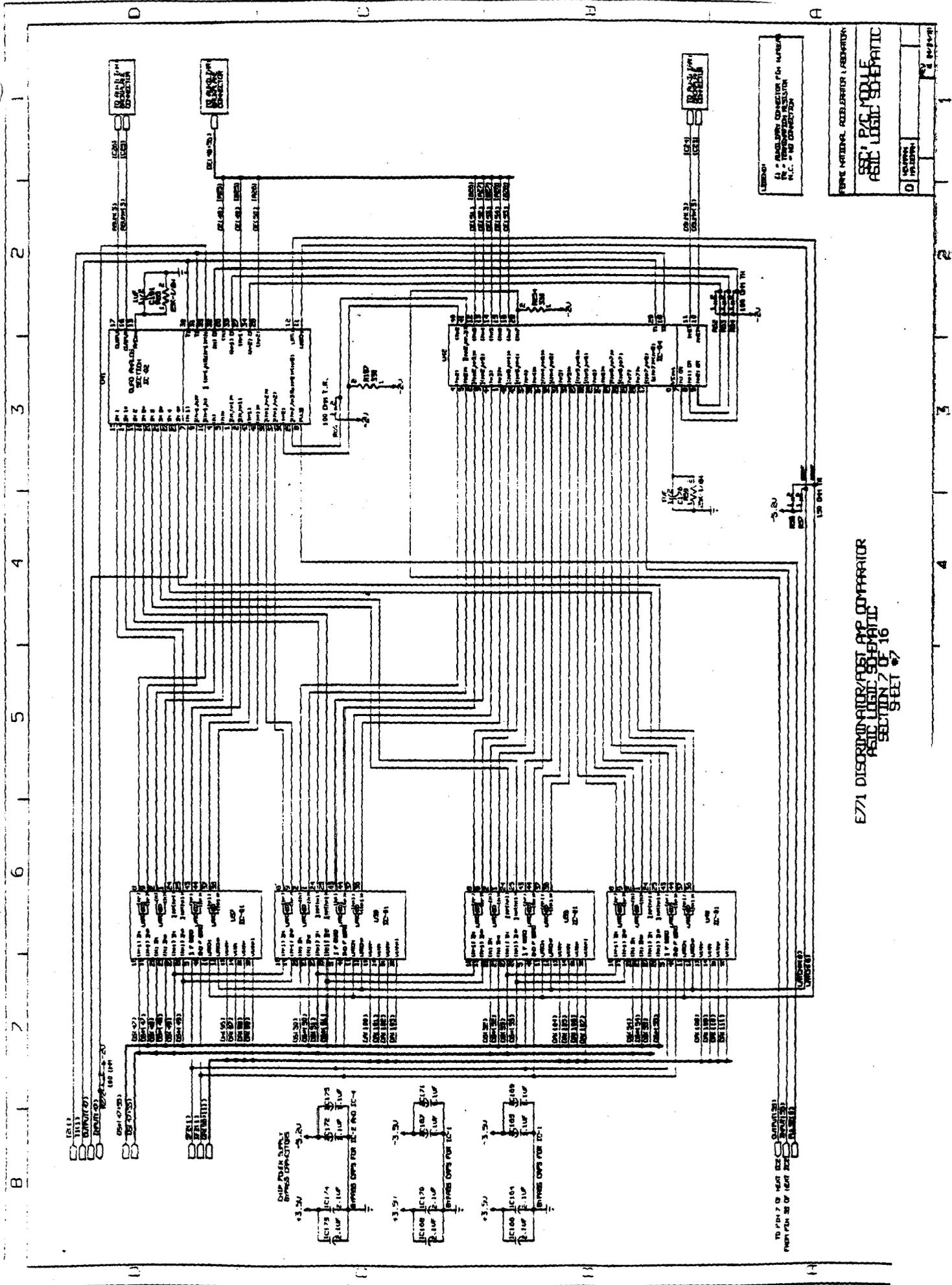
VERSION	NOTES	SHEET #
A		
B		
C		
D		
E		
F	REVERSED INPUTS TO U186 AND CHANGED TO DAC READ	24
G	SWAPPED LABELS FOR E/B AUX CONN C14 & C15	21
H	REMOVED ANALOG GROUND FROM GROUND CONNECTIONS AND REMOVED GROUND FROM F/B AUX CONN C50 ADDED C10	25
I	ADDED GNDS C9, C30, C49, C50 C62, C63	21
J	ADDED DELAY CIRCUITRY AND ROTARY SWITCH MODIFIED LED DRIVER	21
K	CHANGED RESISTORS FROM 100 TO 1.5, 9, 13 50 OHMS AND MODIFIED BUFFER U186	26

E771 DISCRIMINATOR
FASTBUS INTERFACE
CONTROL LOGIC

A NEUMAN HALDAMAN

REV K 04/24/91

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1



E771 DISCRIMINATOR/FIRST AND COMPARETOR
 BASIC LOGIC SCHEMATIC
 SECTION 7 OF 16
 SHEET #7

LIBRARY
 1. ANALOGY CONNECTOR FOR MAPPING
 IN - TRANSDUCION RESOLUTION
 N.C. - NO CONNECTION

FORM NATIONAL ACCELERATOR LABORATORY
 SSC, P/C MODULE
 BASIC LOGIC SCHEMATIC
 01
 10/10/71

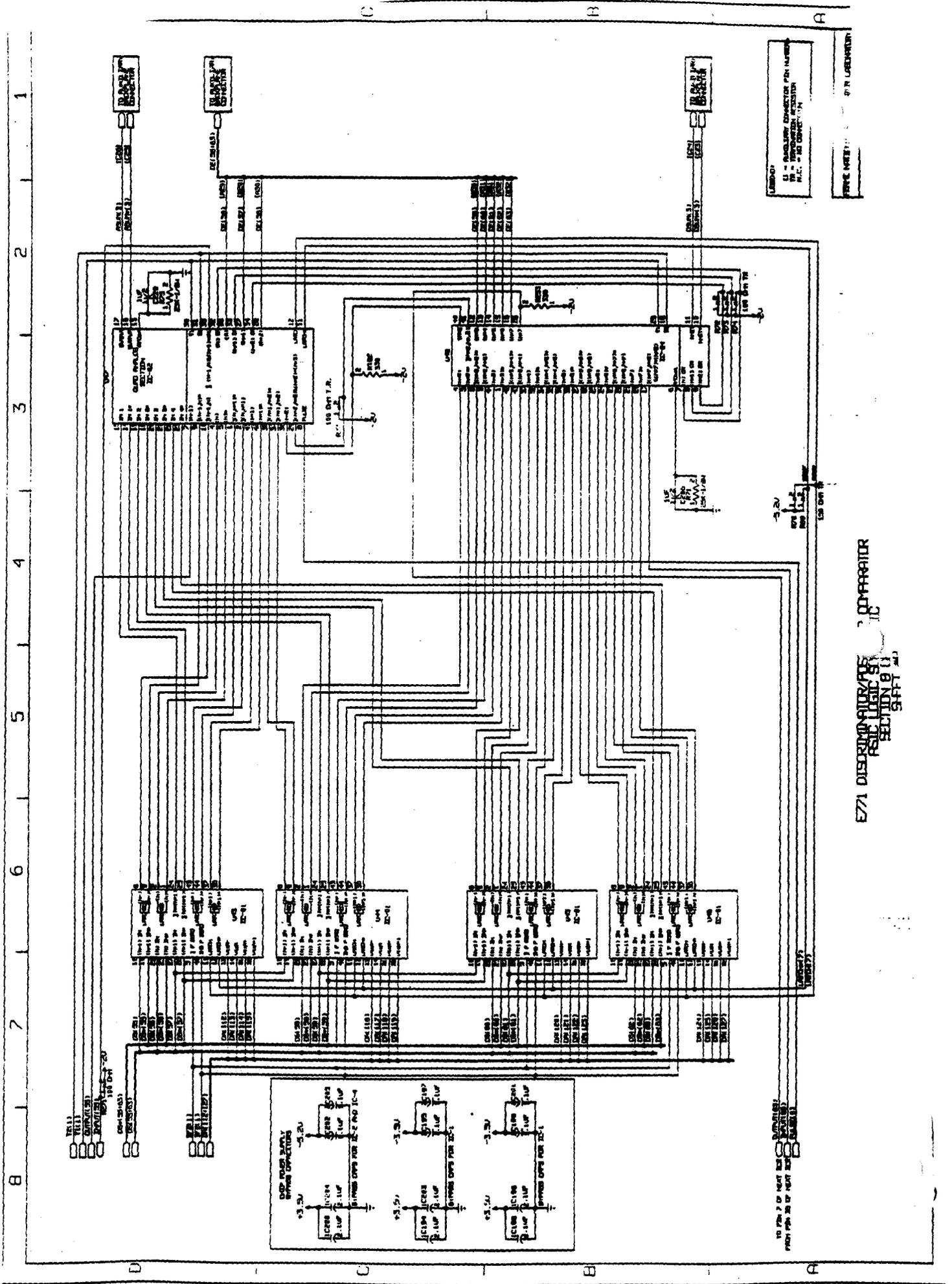
TO PIN 7 OF 7404 OR 7402 OR 7401
 POINT TO 30 OF 7404 OR 7402
 (ALL OTHERS)



B 1 2 3 4 5 6 7

1 2 3 4

D C B A

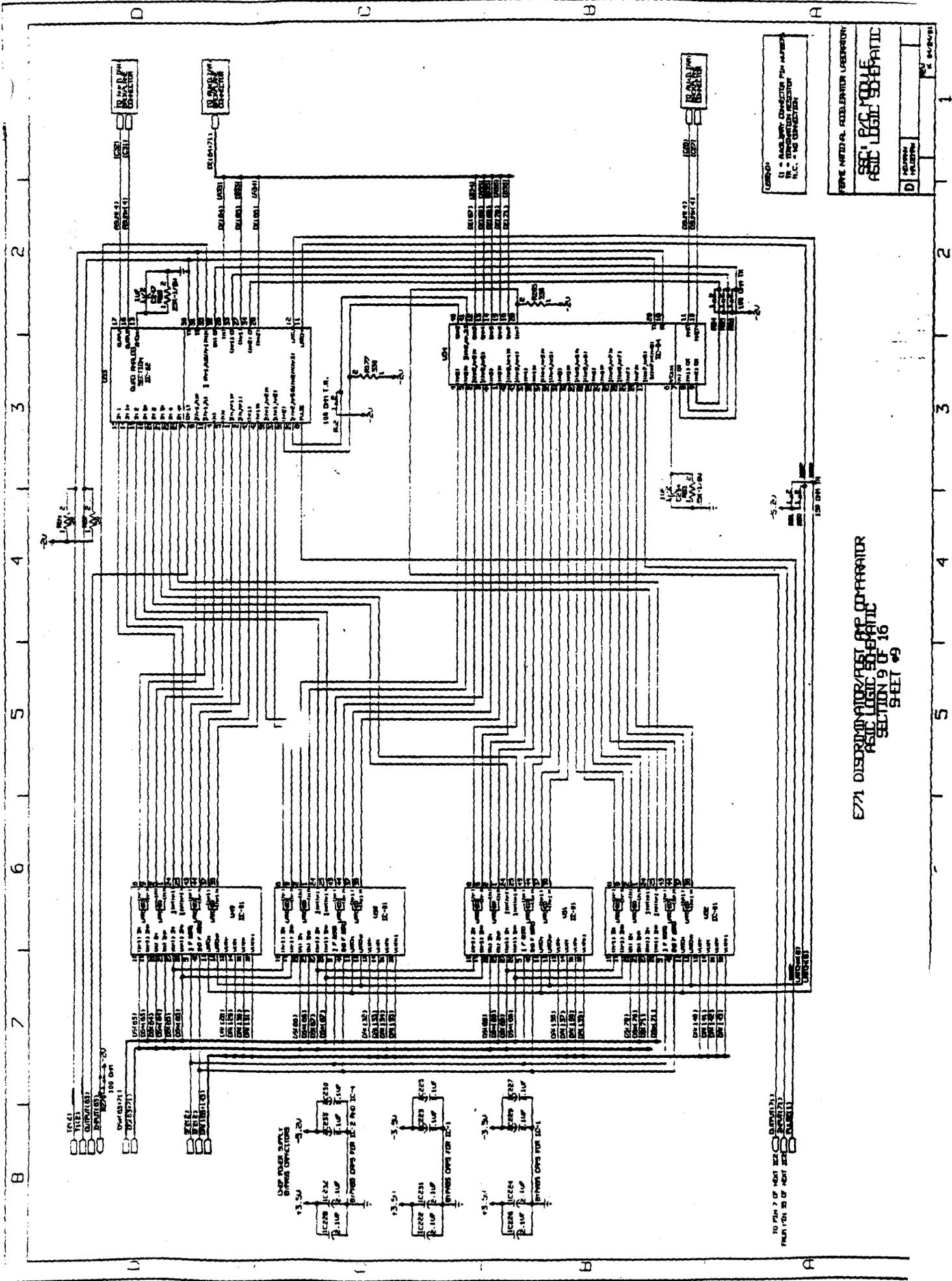


E771 DISCRIMINATOR/POS IC COMPARATOR
 ASIC LOGIC SECTION 011
 PART 2

LEGEND:
 □ PINS WITH CONNECTORS FOR PLACEMENT
 ○ PINS WITH CONNECTORS
 P.W.C. = PIN CONNECTION

NOTE: SEE DRAWING 011 FOR LABELING

TO PIN 7 OF NEXT IC SEE DRAWING
 PRINT PIN 20 OF NEXT IC SEE DRAWING

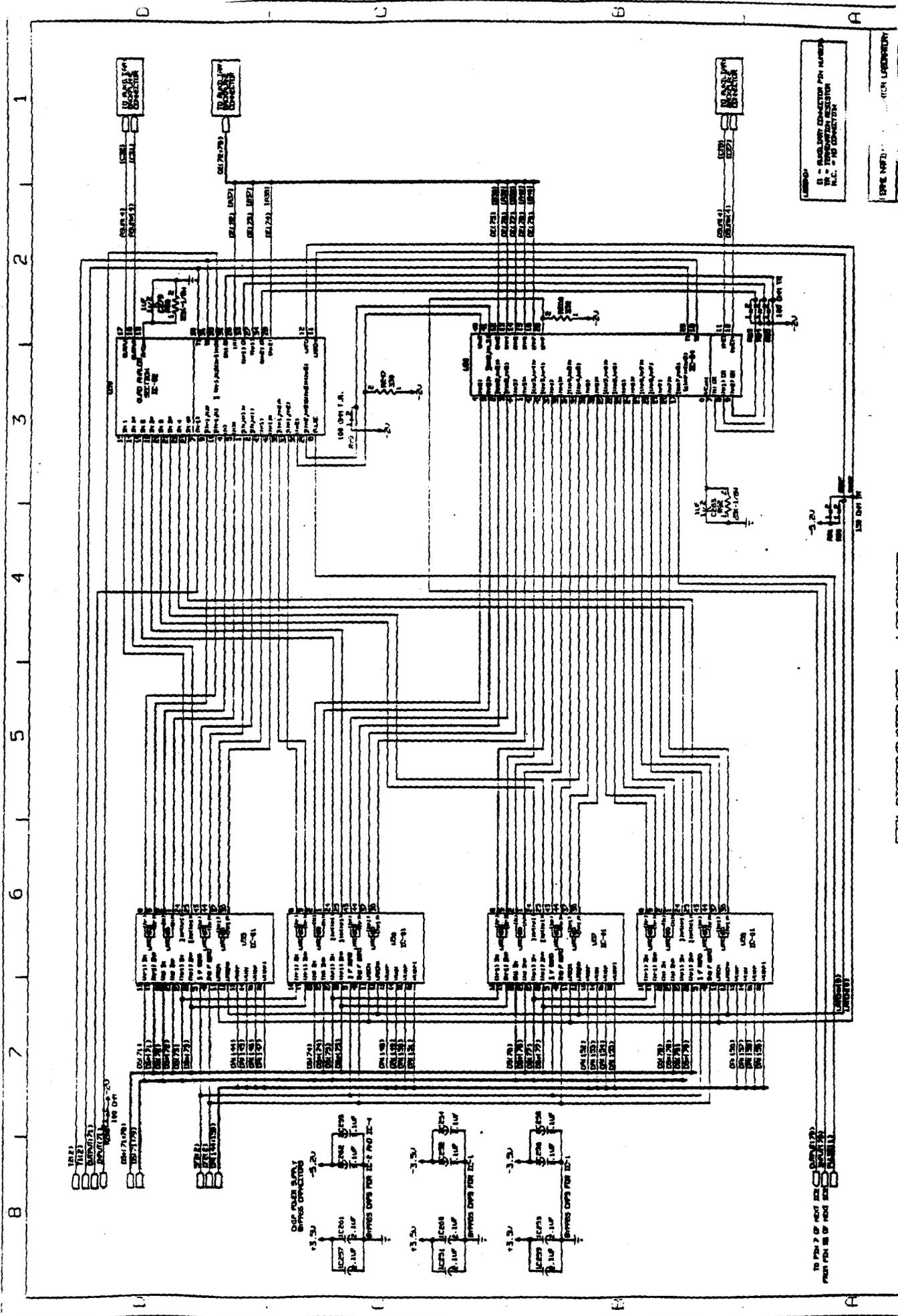


E771 DISCRIMINATOR/PULSE RATE COMPARATOR
 BASIC LOGIC SCHEMATIC
 SECTION 9 OF 16
 SHEET #9

U = ASSEMBLY CONNECTOR PIN HEADER
 N.C. = NO CONNECTION

TRAC: []
 DATE: []
 TITLE: []
 SHEET: []

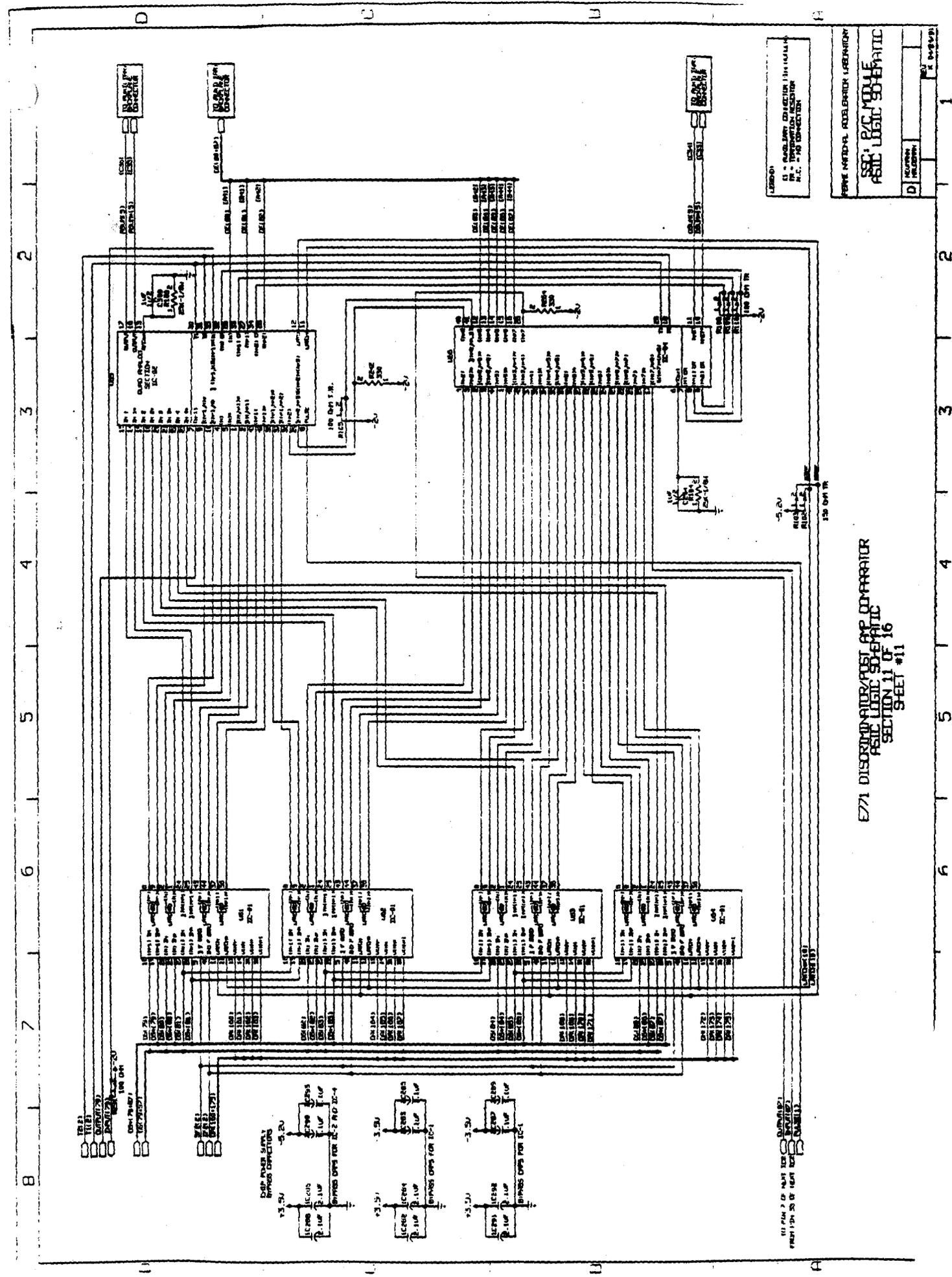
TO PIN 7 OF MOST 222 (PART 121)
 FROM PIN 20 OF MOST 222 (PART 121)



U1880
 74181 ALU
 U1881
 74181 ALU
 U1882
 74181 ALU
 U1883
 74181 ALU

771 DISCRETE LOGIC ALU COMPARATOR
 BASIC LOGIC SECTION 10.11
 8/67

TO PIN 2 OF EACH U1, U2, U3, U4
 FROM PIN 10 OF EACH U1, U2, U3, U4

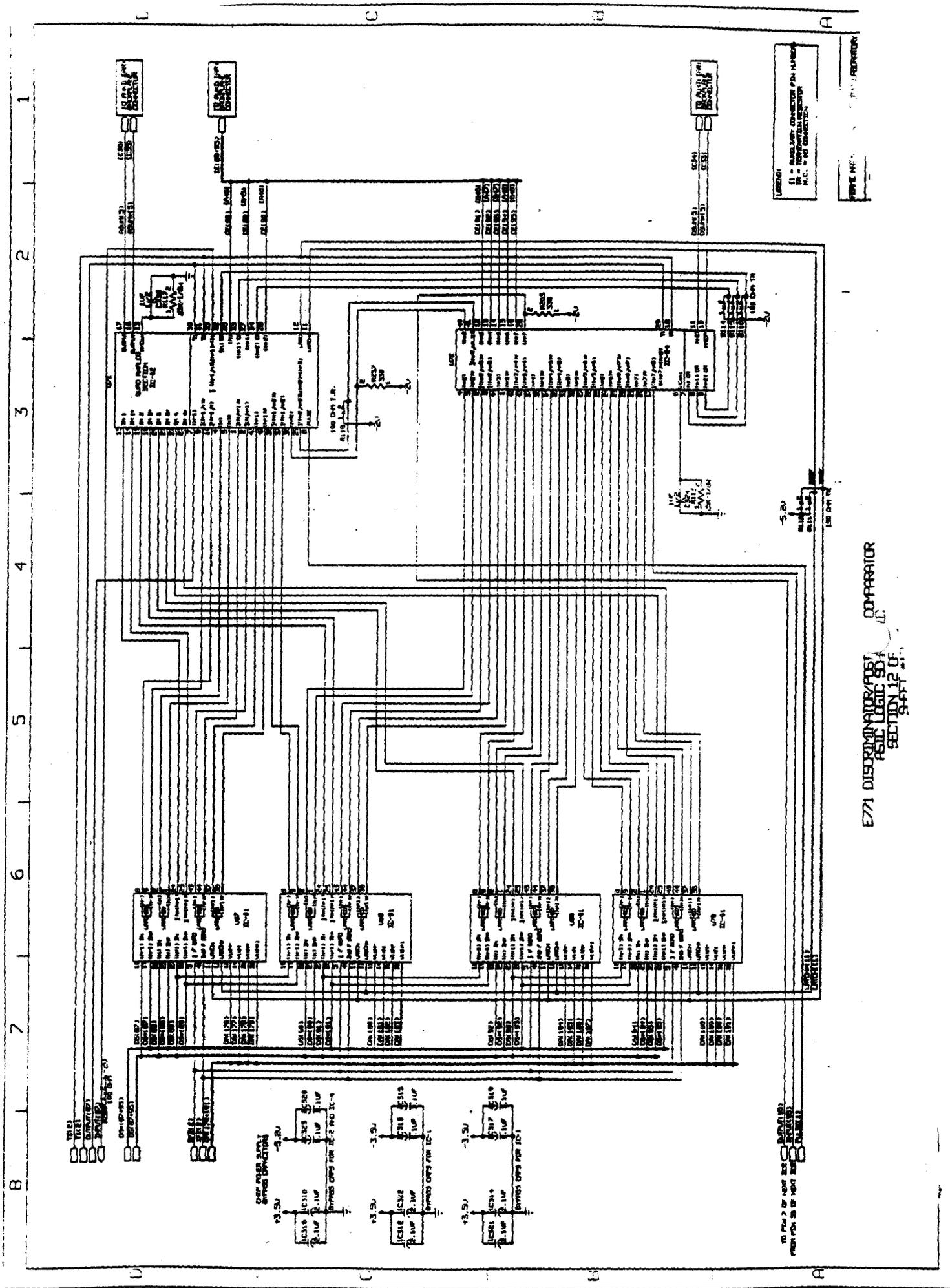


E771 DISCRIMINATOR/POST AMP COMPARATOR
 ASIC LOGIC SCHEMATIC
 SECTION 11 OF 16
 SHEET #11

DESIGNED BY: [Name]
 DRAWN BY: [Name]
 CHECKED BY: [Name]
 DATE: [Date]

PERFORMED BY: [Name]
 DATE: [Date]
 APPROVED BY: [Name]

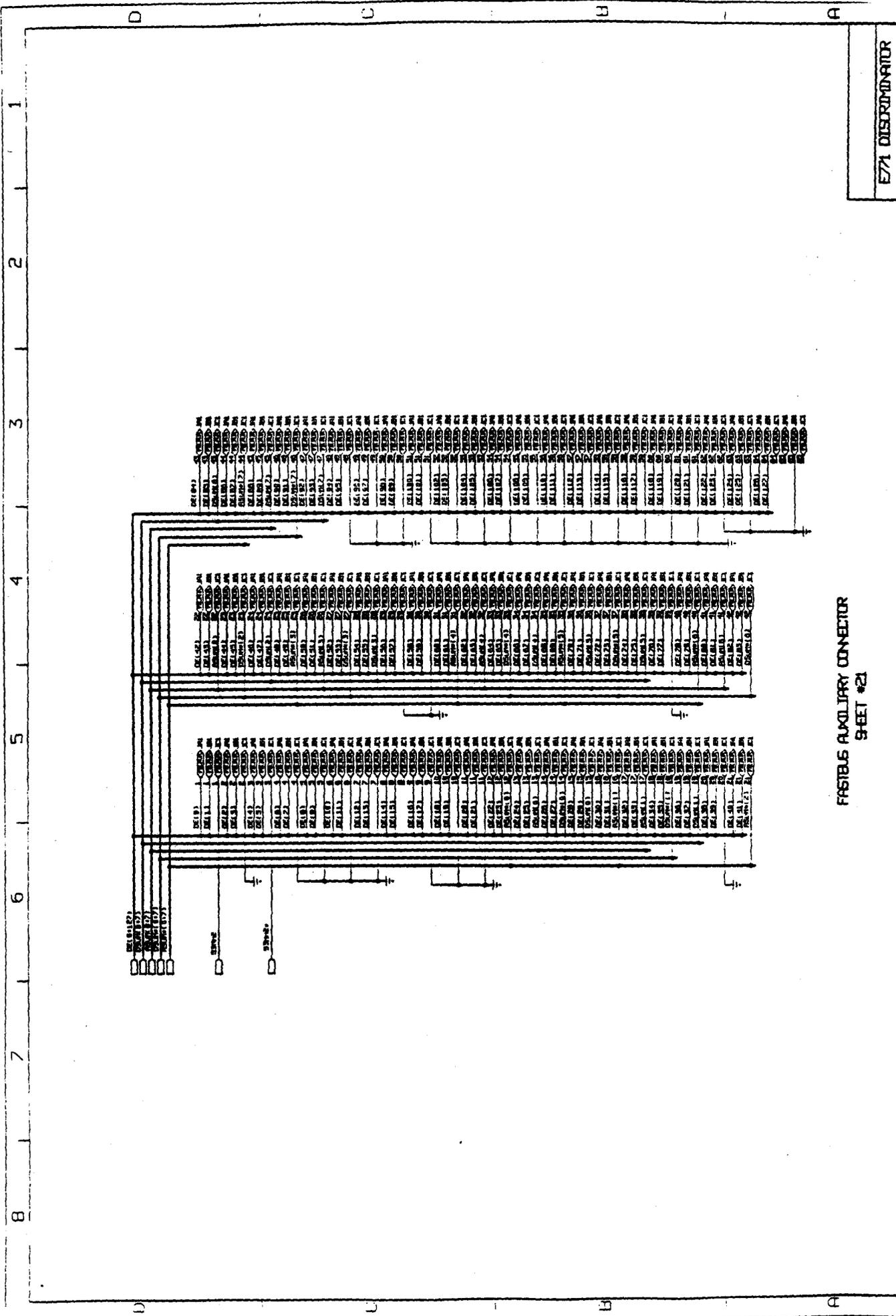
(1) PART 2 OF PART 1000 (DISCRIMINATOR/POST AMP COMPARATOR) IS ON SHEET #10 OF PART 1000 (DISCRIMINATOR/POST AMP COMPARATOR)



(LEGEND)
 11 - STANDARD COMPONENT PIN NUMBER
 N.C. - NOT CONNECTED
 NONE ME. - NONE MEASURED

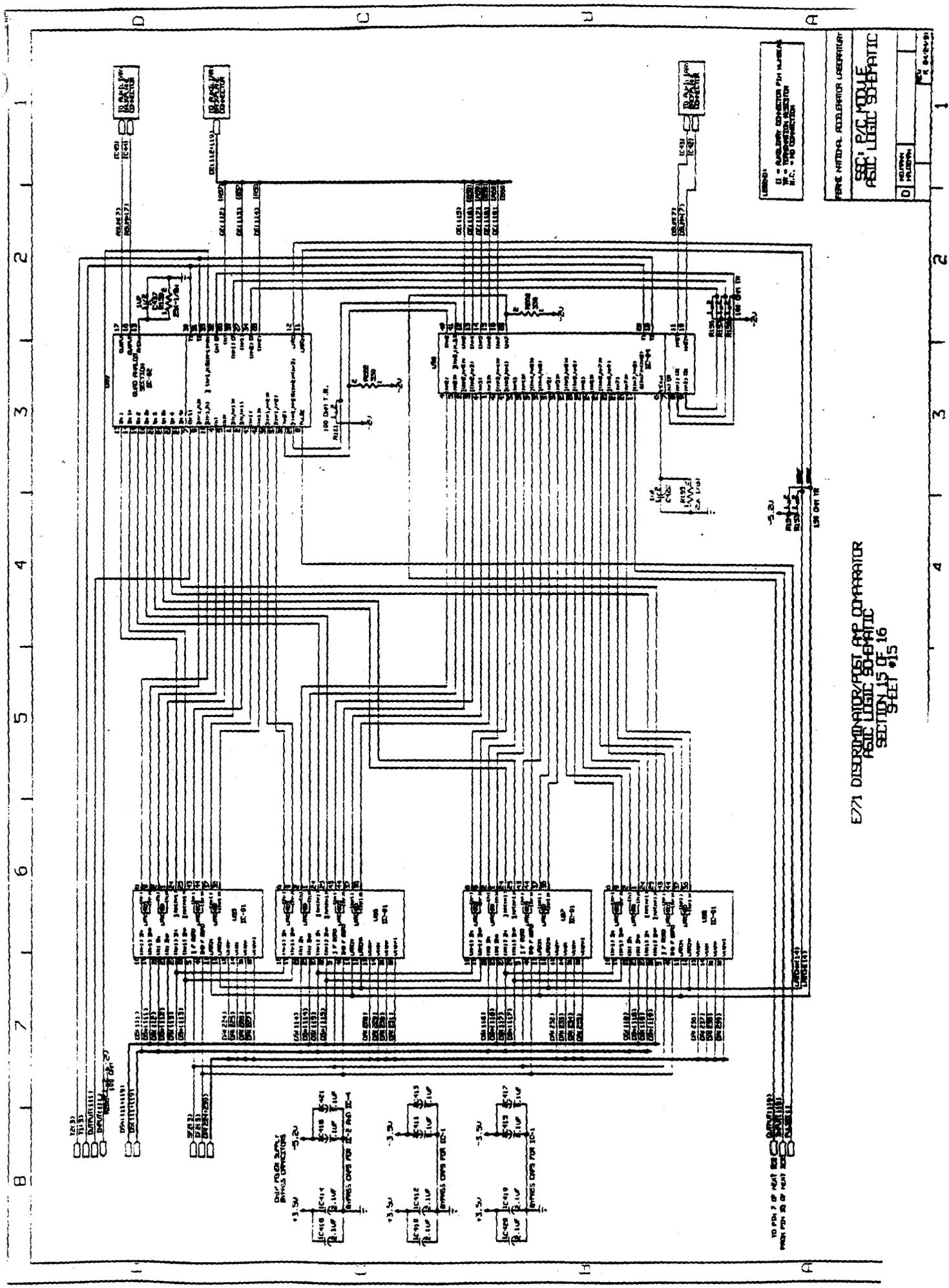
E71 DISCRIMINATOR POST PULSE LOGIC BOARD
 SECTION 12 OF 34

TO PIN 2 OF NEXT BOARD
 FROM PIN 20 OF NEXT BOARD



FASTBUS AUXILIARY CONNECTOR
SHEET #21

E71 DISCRIMINATOR	
FASTBUS AUXILIARY CONNECTOR	
REVISED	DATE
0	11/11/81



E771 DISCRIMINATOR/POST AMP COMPARETOR
 BASIC LOGIC SCHEMATIC
 SECTION 15 OF 16
 SHEET #15

LEGEND:
 □ = BUS CONNECTION FOR POWER SUPPLY
 □ = BUS CONNECTION

PERMITS NATIONAL ACCELERATOR LABORATORY
 SSC FAC MODULE
 BASIC LOGIC SCHEMATIC
 D 15 OF 16
 SHEET #15

TO PIN 2 OF HEAT SINK FOR IC-101
 FROM PIN 15 OF HEAT SINK FOR IC-101



1 2 3 4 5 6 7 8

1 2 3 4

D

C

B

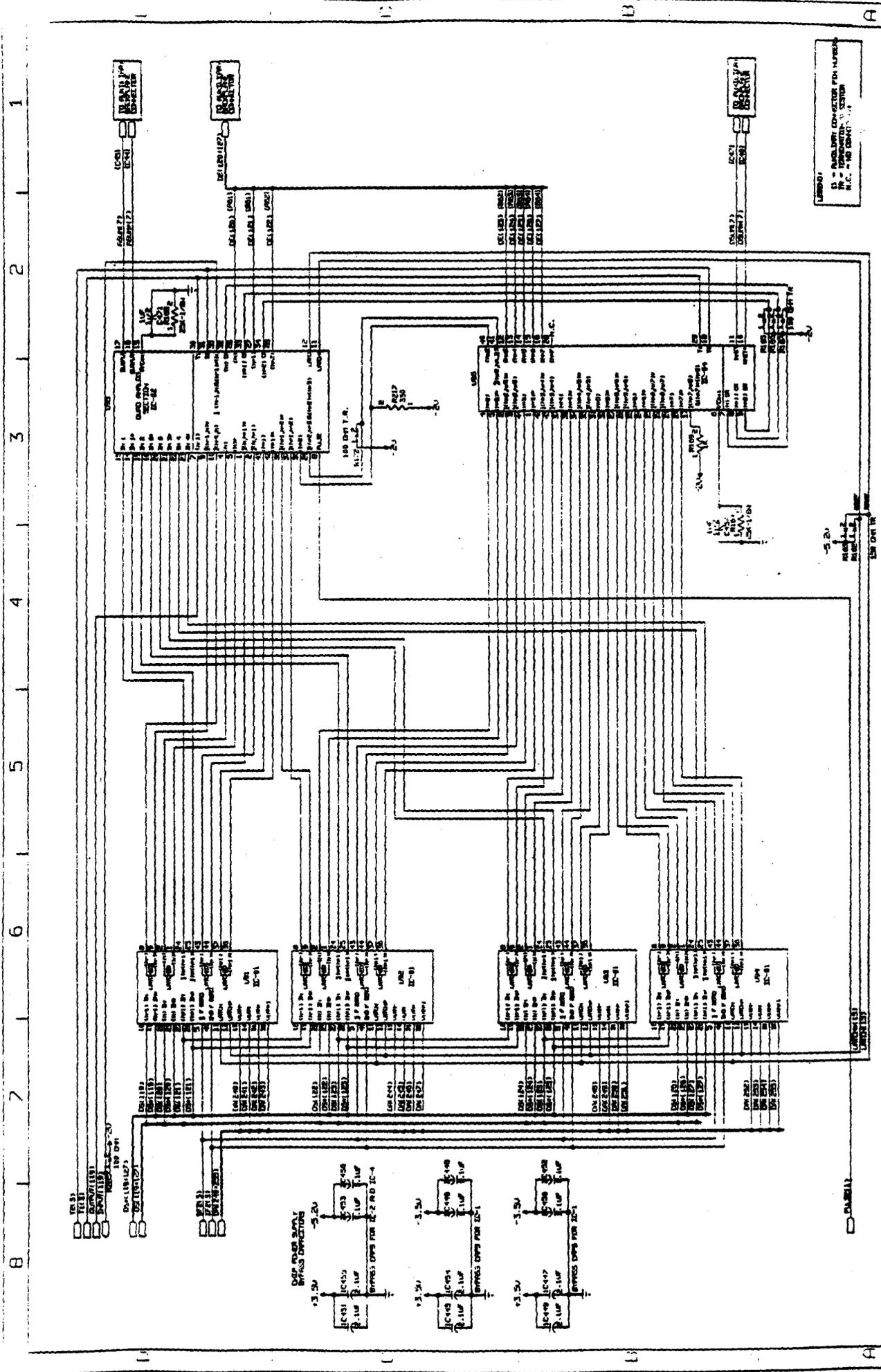
A

A

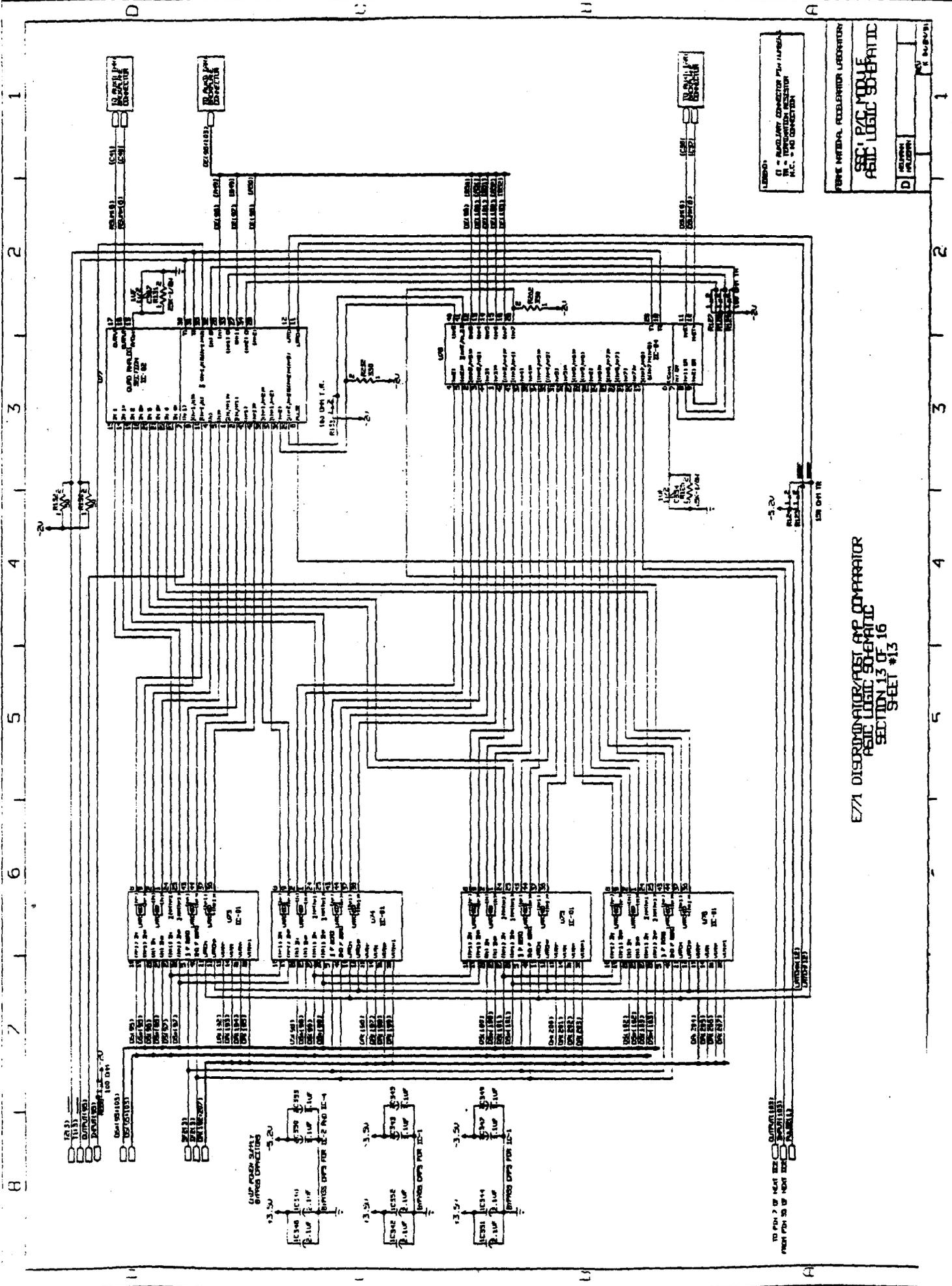
B

C

D



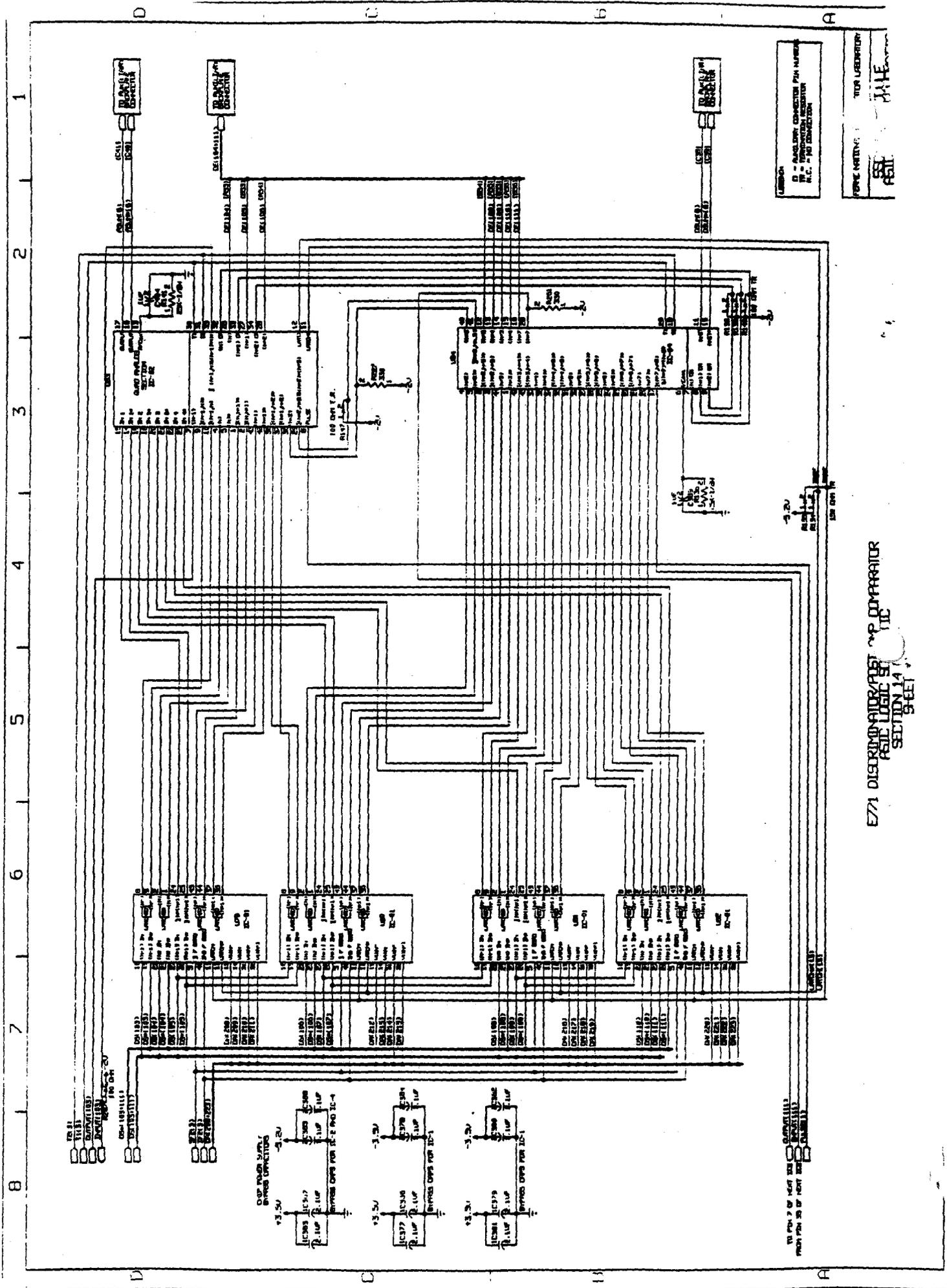
E771 DISCRIMINATOR/FUEL LOGIC SECTION 16 OF 17



E771 DISCRIMINATOR/POST AMP COMPARATOR
 ASIC LOGIC SCHEMATIC
 SECTION 13 OF 16
 SHEET #13

FORMER MEDIA RESEARCH LABORATORY
 ASIC LOGIC SCHEMATIC
 D
 100MILL

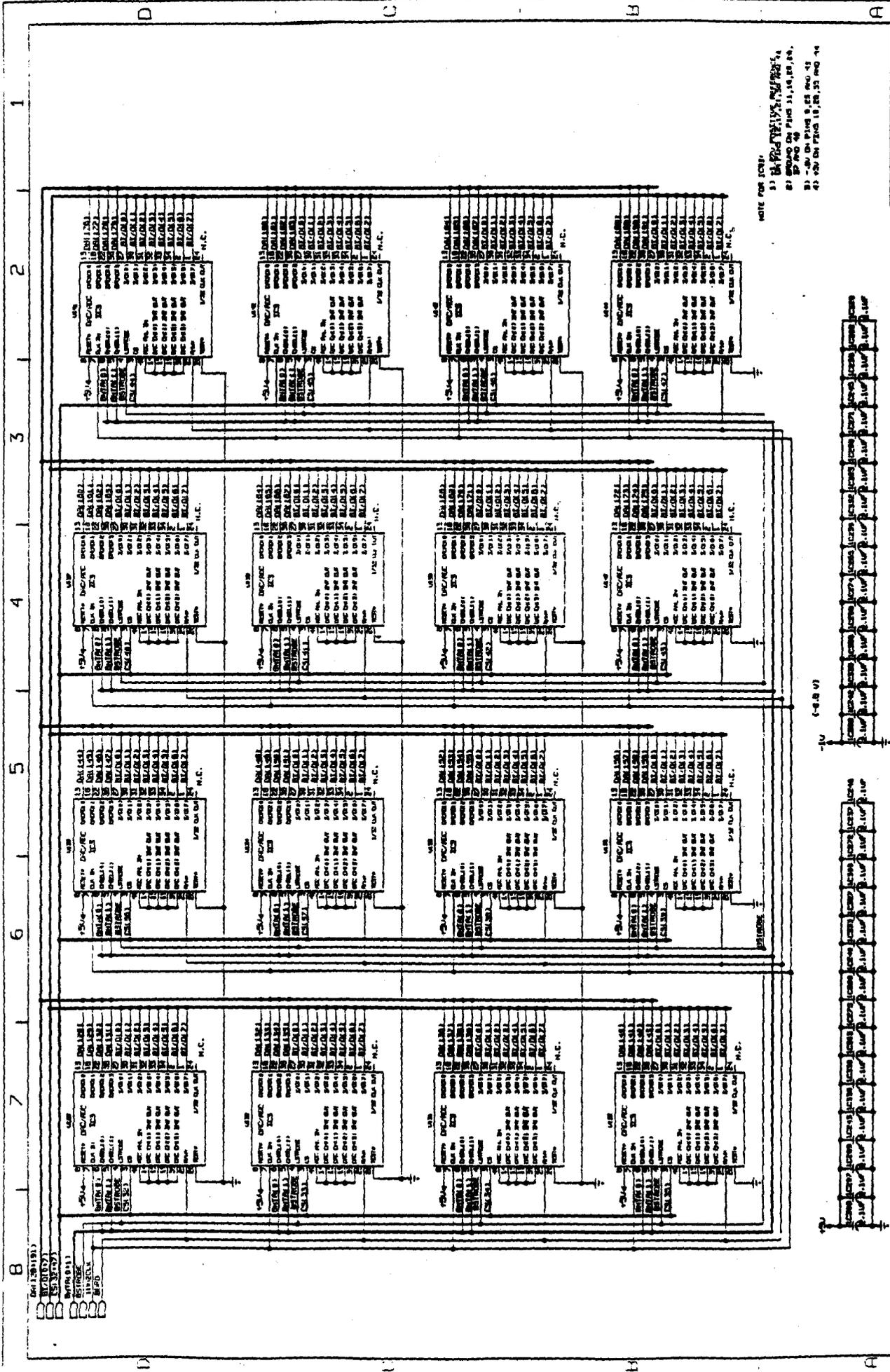
TO PIN 2 OF HEAT SINK QUANTITY 100
 PARTS PER 50 OF 100T SIZE 100MILL



D - ANALOGY CONNECTOR PIN NUMBER
 R - ANALOGY RESISTOR
 C - ANALOGY CAPACITOR

E771 DISCRIMINATOR/FIRST OVER COMPARTOR
 PURE LOGIC 5
 SECTION 14
 SHEET 9

TO PIN 7 OF IC337
 TO PIN 2 OF IC338
 TO PIN 2 OF IC339
 TO PIN 7 OF IC336
 TO PIN 2 OF IC337
 TO PIN 2 OF IC338
 TO PIN 2 OF IC339

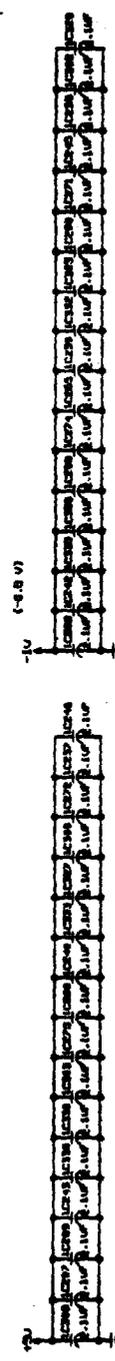


NOTE FOR J081:
 1) BA-124-115, 124-116, 124-117, 124-118, 124-119, 124-120, 124-121, 124-122, 124-123, 124-124, 124-125, 124-126, 124-127, 124-128, 124-129, 124-130, 124-131, 124-132, 124-133, 124-134, 124-135, 124-136, 124-137, 124-138, 124-139, 124-140, 124-141, 124-142, 124-143, 124-144, 124-145, 124-146, 124-147, 124-148, 124-149, 124-150, 124-151, 124-152, 124-153, 124-154, 124-155, 124-156, 124-157, 124-158, 124-159, 124-160, 124-161, 124-162, 124-163, 124-164, 124-165, 124-166, 124-167, 124-168, 124-169, 124-170, 124-171, 124-172, 124-173, 124-174, 124-175, 124-176, 124-177, 124-178, 124-179, 124-180, 124-181, 124-182, 124-183, 124-184, 124-185, 124-186, 124-187, 124-188, 124-189, 124-190, 124-191, 124-192, 124-193, 124-194, 124-195, 124-196, 124-197, 124-198, 124-199, 124-200, 124-201, 124-202, 124-203, 124-204, 124-205, 124-206, 124-207, 124-208, 124-209, 124-210, 124-211, 124-212, 124-213, 124-214, 124-215, 124-216, 124-217, 124-218, 124-219, 124-220, 124-221, 124-222, 124-223, 124-224, 124-225, 124-226, 124-227, 124-228, 124-229, 124-230, 124-231, 124-232, 124-233, 124-234, 124-235, 124-236, 124-237, 124-238, 124-239, 124-240, 124-241, 124-242, 124-243, 124-244, 124-245, 124-246, 124-247, 124-248, 124-249, 124-250, 124-251, 124-252, 124-253, 124-254, 124-255, 124-256, 124-257, 124-258, 124-259, 124-260, 124-261, 124-262, 124-263, 124-264, 124-265, 124-266, 124-267, 124-268, 124-269, 124-270, 124-271, 124-272, 124-273, 124-274, 124-275, 124-276, 124-277, 124-278, 124-279, 124-280, 124-281, 124-282, 124-283, 124-284, 124-285, 124-286, 124-287, 124-288, 124-289, 124-290, 124-291, 124-292, 124-293, 124-294, 124-295, 124-296, 124-297, 124-298, 124-299, 124-300, 124-301, 124-302, 124-303, 124-304, 124-305, 124-306, 124-307, 124-308, 124-309, 124-310, 124-311, 124-312, 124-313, 124-314, 124-315, 124-316, 124-317, 124-318, 124-319, 124-320, 124-321, 124-322, 124-323, 124-324, 124-325, 124-326, 124-327, 124-328, 124-329, 124-330, 124-331, 124-332, 124-333, 124-334, 124-335, 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124-669, 124-670, 124-671, 124-672, 124-673, 124-674, 124-675, 124-676, 124-677, 124-678, 124-679, 124-680, 124-681, 124-682, 124-683, 124-684, 124-685, 124-686, 124-687, 124-688, 124-689, 124-690, 124-691, 124-692, 124-693, 124-694, 124-695, 124-696, 124-697, 124-698, 124-699, 124-700, 124-701, 124-702, 124-703, 124-704, 124-705, 124-706, 124-707, 124-708, 124-709, 124-710, 124-711, 124-712, 124-713, 124-714, 124-715, 124-716, 124-717, 124-718, 124-719, 124-720, 124-721, 124-722, 124-723, 124-724, 124-725, 124-726, 124-727, 124-728, 124-729, 124-730, 124-731, 124-732, 124-733, 124-734, 124-735, 124-736, 124-737, 124-738, 124-739, 124-740, 124-741, 124-742, 124-743, 124-744, 124-745, 124-746, 124-747, 124-748, 124-749, 124-750, 124-751, 124-752, 124-753, 124-754, 124-755, 124-756, 124-757, 124-758, 124-759, 124-760, 124-761, 124-762, 124-763, 124-764, 124-765, 124-766, 124-767, 124-768, 124-769, 124-770, 124-771, 124-772, 124-773, 124-774, 124-775, 124-776, 124-777, 124-778, 124-779, 124-780, 124-781, 124-782, 124-783, 124-784, 124-785, 124-786, 124-787, 124-788, 124-789, 124-790, 124-791, 124-792, 124-793, 124-794, 124-795, 124-796, 124-797, 124-798, 124-799, 124-800, 124-801, 124-802, 124-803, 124-804, 124-805, 124-806, 124-807, 124-808, 124-809, 124-810, 124-811, 124-812, 124-813, 124-814, 124-815, 124-816, 124-817, 124-818, 124-819, 124-820, 124-821, 124-822, 124-823, 124-824, 124-825, 124-826, 124-827, 124-828, 124-829, 124-830, 124-831, 124-832, 124-833, 124-834, 124-835, 124-836, 124-837, 124-838, 124-839, 124-840, 124-841, 124-842, 124-843, 124-844, 124-845, 124-846, 124-847, 124-848, 124-849, 124-850, 124-851, 124-852, 124-853, 124-854, 124-855, 124-856, 124-857, 124-858, 124-859, 124-860, 124-861, 124-862, 124-863, 124-864, 124-865, 124-866, 124-867, 124-868, 124-869, 124-870, 124-871, 124-872, 124-873, 124-874, 124-875, 124-876, 124-877, 124-878, 124-879, 124-880, 124-881, 124-882, 124-883, 124-884, 124-885, 124-886, 124-887, 124-888, 124-889, 124-890, 124-891, 124-892, 124-893, 124-894, 124-895, 124-896, 124-897, 124-898, 124-899, 124-900, 124-901, 124-902, 124-903, 124-904, 124-905, 124-906, 124-907, 124-908, 124-909, 124-910, 124-911, 124-912, 124-913, 124-914, 124-915, 124-916, 124-917, 124-918, 124-919, 124-920, 124-921, 124-922, 124-923, 124-924, 124-925, 124-926, 124-927, 124-928, 124-929, 124-930, 124-931, 124-932, 124-933, 124-934, 124-935, 124-936, 124-937, 124-938, 124-939, 124-940, 124-941, 124-942, 124-943, 124-944, 124-945, 124-946, 124-947, 124-948, 124-949, 124-950, 124-951, 124-952, 124-953, 124-954, 124-955, 124-956, 124-957, 124-958, 124-959, 124-960, 124-961, 124-962, 124-963, 124-964, 124-965, 124-966, 124-967, 124-968, 124-969, 124-970, 124-971, 124-972, 124-973, 124-974, 124-975, 124-976, 124-977, 124-978, 124-979, 124-980, 124-981, 124-982, 124-983, 124-984, 124-985, 124-986, 124-987, 124-988, 124-989, 124-990, 124-991, 124-992, 124-993, 124-994, 124-995, 124-996, 124-997, 124-998, 124-999, 124-1000.

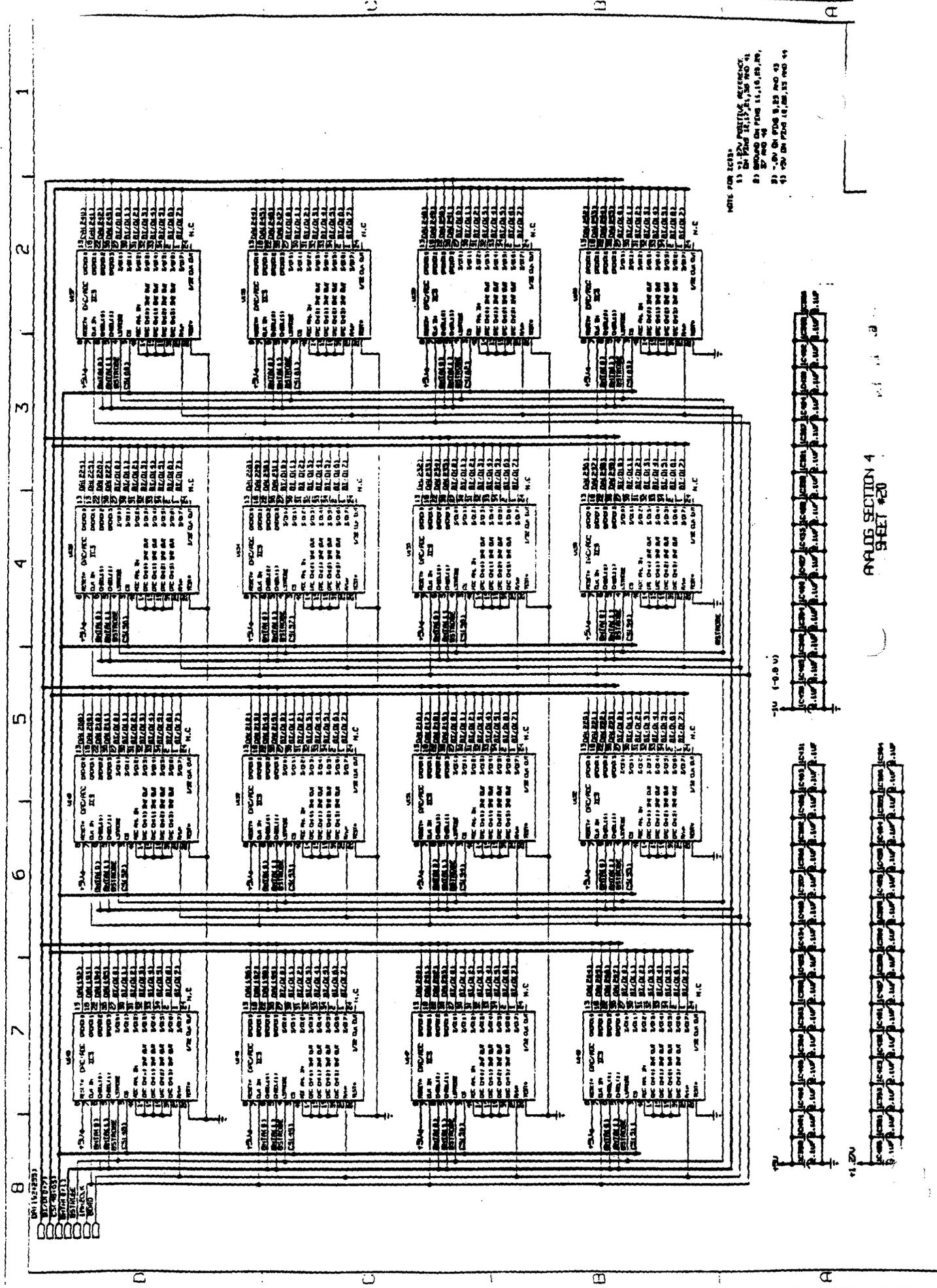
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ANALOG SECTION 3
 SHEET #19

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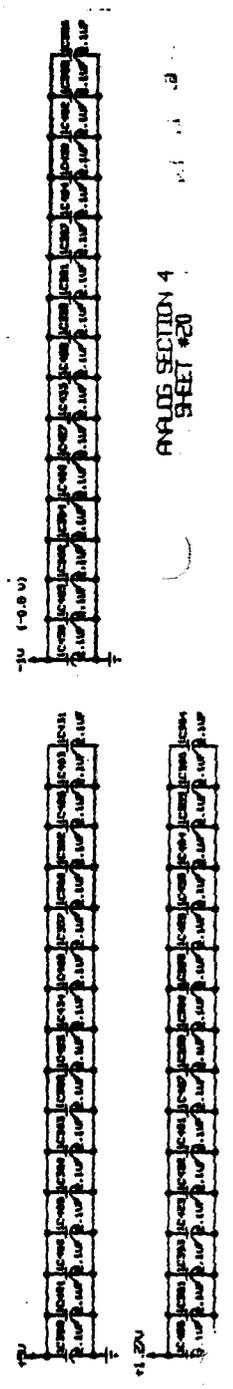


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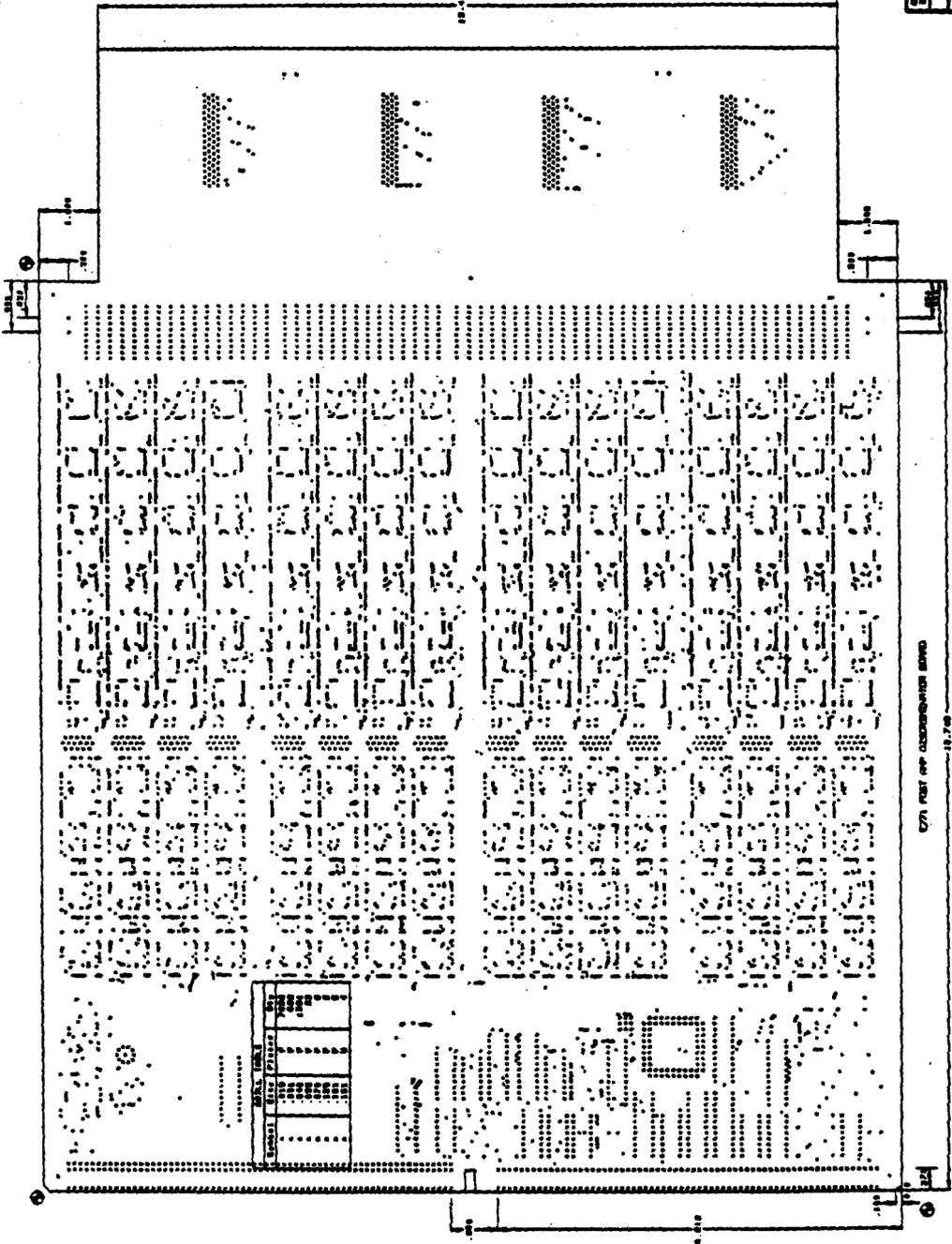


NOTE FOR 10181
 1) 2) 3) 4) 5) 6) 7) 8) 9) 10) 11) 12) 13) 14) 15) 16) 17) 18) 19) 20) 21) 22) 23) 24) 25) 26) 27) 28) 29) 30) 31) 32) 33) 34) 35) 36) 37) 38) 39) 40) 41) 42) 43) 44) 45) 46) 47) 48) 49) 50) 51) 52) 53) 54) 55) 56) 57) 58) 59) 60) 61) 62) 63) 64) 65) 66) 67) 68) 69) 70) 71) 72) 73) 74) 75) 76) 77) 78) 79) 80) 81) 82) 83) 84) 85) 86) 87) 88) 89) 90) 91) 92) 93) 94) 95) 96) 97) 98) 99) 100) 101) 102) 103) 104) 105) 106) 107) 108) 109) 110) 111) 112) 113) 114) 115) 116) 117) 118) 119) 120) 121) 122) 123) 124) 125) 126) 127) 128) 129) 130) 131) 132) 133) 134) 135) 136) 137) 138) 139) 140) 141) 142) 143) 144) 145) 146) 147) 148) 149) 150) 151) 152) 153) 154) 155) 156) 157) 158) 159) 160) 161) 162) 163) 164) 165) 166) 167) 168) 169) 170) 171) 172) 173) 174) 175) 176) 177) 178) 179) 180) 181) 182) 183) 184) 185) 186) 187) 188) 189) 190) 191) 192) 193) 194) 195) 196) 197) 198) 199) 200) 201) 202) 203) 204) 205) 206) 207) 208) 209) 210) 211) 212) 213) 214) 215) 216) 217) 218) 219) 220) 221) 222) 223) 224) 225) 226) 227) 228) 229) 230) 231) 232) 233) 234) 235) 236) 237) 238) 239) 240) 241) 242) 243) 244) 245) 246) 247) 248) 249) 250) 251) 252) 253) 254) 255) 256) 257) 258) 259) 260) 261) 262) 263) 264) 265) 266) 267) 268) 269) 270) 271) 272) 273) 274) 275) 276) 277) 278) 279) 280) 281) 282) 283) 284) 285) 286) 287) 288) 289) 290) 291) 292) 293) 294) 295) 296) 297) 298) 299) 300) 301) 302) 303) 304) 305) 306) 307) 308) 309) 310) 311) 312) 313) 314) 315) 316) 317) 318) 319) 320) 321) 322) 323) 324) 325) 326) 327) 328) 329) 330) 331) 332) 333) 334) 335) 336) 337) 338) 339) 340) 341) 342) 343) 344) 345) 346) 347) 348) 349) 350) 351) 352) 353) 354) 355) 356) 357) 358) 359) 360) 361) 362) 363) 364) 365) 366) 367) 368) 369) 370) 371) 372) 373) 374) 375) 376) 377) 378) 379) 380) 381) 382) 383) 384) 385) 386) 387) 388) 389) 390) 391) 392) 393) 394) 395) 396) 397) 398) 399) 400) 401) 402) 403) 404) 405) 406) 407) 408) 409) 410) 411) 412) 413) 414) 415) 416) 417) 418) 419) 420) 421) 422) 423) 424) 425) 426) 427) 428) 429) 430) 431) 432) 433) 434) 435) 436) 437) 438) 439) 440) 441) 442) 443) 444) 445) 446) 447) 448) 449) 450) 451) 452) 453) 454) 455) 456) 457) 458) 459) 460) 461) 462) 463) 464) 465) 466) 467) 468) 469) 470) 471) 472) 473) 474) 475) 476) 477) 478) 479) 480) 481) 482) 483) 484) 485) 486) 487) 488) 489) 490) 491) 492) 493) 494) 495) 496) 497) 498) 499) 500) 501) 502) 503) 504) 505) 506) 507) 508) 509) 510) 511) 512) 513) 514) 515) 516) 517) 518) 519) 520) 521) 522) 523) 524) 525) 526) 527) 528) 529) 530) 531) 532) 533) 534) 535) 536) 537) 538) 539) 540) 541) 542) 543) 544) 545) 546) 547) 548) 549) 550) 551) 552) 553) 554) 555) 556) 557) 558) 559) 560) 561) 562) 563) 564) 565) 566) 567) 568) 569) 570) 571) 572) 573) 574) 575) 576) 577) 578) 579) 580) 581) 582) 583) 584) 585) 586) 587) 588) 589) 590) 591) 592) 593) 594) 595) 596) 597) 598) 599) 600) 601) 602) 603) 604) 605) 606) 607) 608) 609) 610) 611) 612) 613) 614) 615) 616) 617) 618) 619) 620) 621) 622) 623) 624) 625) 626) 627) 628) 629) 630) 631) 632) 633) 634) 635) 636) 637) 638) 639) 640) 641) 642) 643) 644) 645) 646) 647) 648) 649) 650) 651) 652) 653) 654) 655) 656) 657) 658) 659) 660) 661) 662) 663) 664) 665) 666) 667) 668) 669) 670) 671) 672) 673) 674) 675) 676) 677) 678) 679) 680) 681) 682) 683) 684) 685) 686) 687) 688) 689) 690) 691) 692) 693) 694) 695) 696) 697) 698) 699) 700) 701) 702) 703) 704) 705) 706) 707) 708) 709) 710) 711) 712) 713) 714) 715) 716) 717) 718) 719) 720) 721) 722) 723) 724) 725) 726) 727) 728) 729) 730) 731) 732) 733) 734) 735) 736) 737) 738) 739) 740) 741) 742) 743) 744) 745) 746) 747) 748) 749) 750) 751) 752) 753) 754) 755) 756) 757) 758) 759) 760) 761) 762) 763) 764) 765) 766) 767) 768) 769) 770) 771) 772) 773) 774) 775) 776) 777) 778) 779) 780) 781) 782) 783) 784) 785) 786) 787) 788) 789) 790) 791) 792) 793) 794) 795) 796) 797) 798) 799) 800) 801) 802) 803) 804) 805) 806) 807) 808) 809) 810) 811) 812) 813) 814) 815) 816) 817) 818) 819) 820) 821) 822) 823) 824) 825) 826) 827) 828) 829) 830) 831) 832) 833) 834) 835) 836) 837) 838) 839) 840) 841) 842) 843) 844) 845) 846) 847) 848) 849) 850) 851) 852) 853) 854) 855) 856) 857) 858) 859) 860) 861) 862) 863) 864) 865) 866) 867) 868) 869) 870) 871) 872) 873) 874) 875) 876) 877) 878) 879) 880) 881) 882) 883) 884) 885) 886) 887) 888) 889) 890) 891) 892) 893) 894) 895) 896) 897) 898) 899) 900) 901) 902) 903) 904) 905) 906) 907) 908) 909) 910) 911) 912) 913) 914) 915) 916) 917) 918) 919) 920) 921) 922) 923) 924) 925) 926) 927) 928) 929) 930) 931) 932) 933) 934) 935) 936) 937) 938) 939) 940) 941) 942) 943) 944) 945) 946) 947) 948) 949) 950) 951) 952) 953) 954) 955) 956) 957) 958) 959) 960) 961) 962) 963) 964) 965) 966) 967) 968) 969) 970) 971) 972) 973) 974) 975) 976) 977) 978) 979) 980) 981) 982) 983) 984) 985) 986) 987) 988) 989) 990) 991) 992) 993) 994) 995) 996) 997) 998) 999) 1000)

ANALOG SECTION 4
 SHEET #20



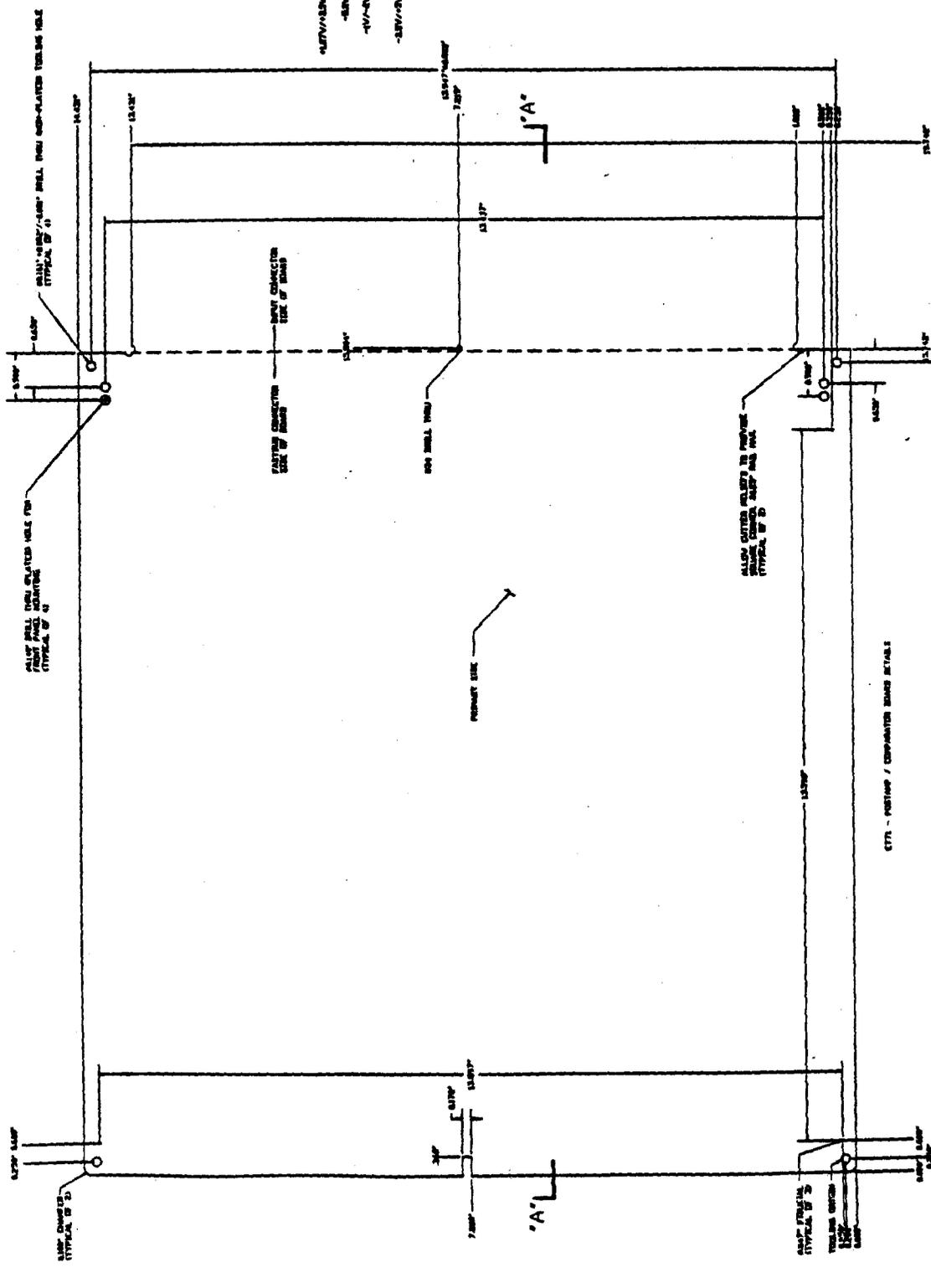
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| 671 POST OFFICE AUTOMATION BOARD | |
| DATE | 10/1/78 |
| REV | 1 |
| DESIGNED BY | ... |
| CHECKED BY | ... |
| APPROVED BY | ... |
| DATE | ... |
| FEDERAL BUREAU OF INVESTIGATION
U.S. DEPARTMENT OF JUSTICE | |
| 777 POST OFFICE AUTOMATION BOARD
PHIL. DELANEY
PHILADELPHIA, PA. 19104 | |

7512

7512



| EASTING CONNECTOR SIDE OF BOARD | | WESTING CONNECTOR SIDE OF BOARD | |
|---------------------------------|--------|---------------------------------|--------|
| PREPREG | 1/4" ± | PREPREG | 1/4" ± |
| CORE | 1/8" ± | CORE | 1/8" ± |
| COPPER | 1/8" ± | COPPER | 1/8" ± |
| PLATED HOLE | 1/2" ± | PLATED HOLE | 1/2" ± |
| NON-PLATED THROUGH HOLE | 1/2" ± | NON-PLATED THROUGH HOLE | 1/2" ± |
| MINI-DRILL/DRILL MILL DRILL | 1/2" ± | MINI-DRILL/DRILL MILL DRILL | 1/2" ± |
| DRILL | 1/2" ± | DRILL | 1/2" ± |

NOTES:

1. BOARD THICKNESS SHALL BE 0.0625" ± 0.0025"
2. DRILL ALL DRILL HOLES ON BOARD
3. VENTURE AND HORIZONTAL STRENGTH FROM PLATING SHALL NOT EXCEED 0.001"
4. HOLE OF BOARD MUST BE NON-CONDUCTIVE SINCE IT CAN TOUCH INSULATION
5. ALL VIAS SHALL BE FILLER WITH 100% FILL INSULATION OVER BOARD COPPER
6. ALL THROUGH HOLE PADS SHALL BE TEMP-STRIPPED
7. ALL PLATED THROUGH HOLES SHALL BE 1/8" DIA.
8. PADS SHALL BE NOT BE LEVELLED FROM-TO-TO
9. FINISHED HOLE TOLERANCE SHALL BE ±0.001"
10. HOLE SIZE SPECIFIED BY DRILL TABLE AND FINISHED HOLE SIZE
11. NON-CONDUCTIVE INSULATION FOR HOLE VISE LAYER A
12. HOLE FOR DRILL HOLE SHALL BE 1/8" DIA.
13. HOLE FOR DRILL HOLE SHALL BE 1/8" DIA.
14. HOLE FOR DRILL HOLE SHALL BE 1/8" DIA.

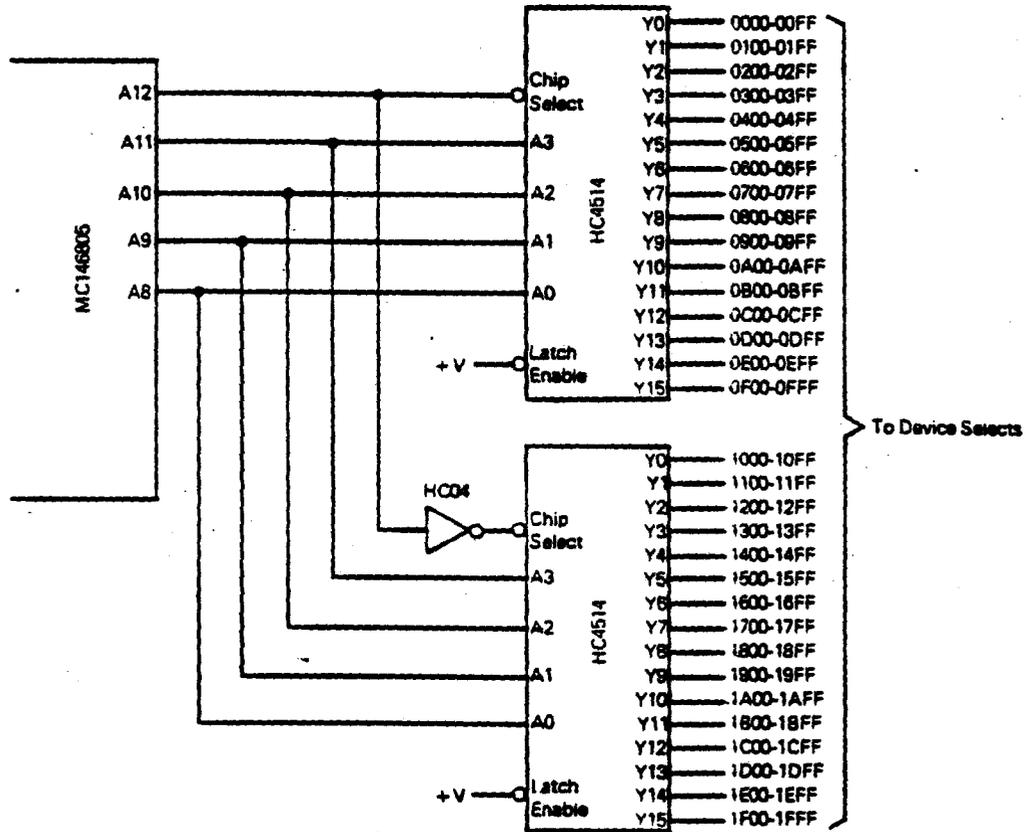
| DESCRIPTION OF BOARD | |
|----------------------|----------------|
| DATE | 1/1/70 |
| DESIGNED BY | J. J. CRISTIAN |
| CHECKED BY | J. J. CRISTIAN |
| APPROVED BY | J. J. CRISTIAN |
| DATE | 1/1/70 |
| DESIGNED BY | J. J. CRISTIAN |
| CHECKED BY | J. J. CRISTIAN |
| APPROVED BY | J. J. CRISTIAN |
| DATE | 1/1/70 |
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| DATE | 1/1/70 |
| DESIGNED BY | J. J. CRISTIAN |
| CHECKED BY | J. J. CRISTIAN |
| APPROVED BY | J. J. CRISTIAN |
| DATE | 1/1/70 |
| DESIGNED BY | J. J. CRISTIAN |
| CHECKED BY | J. J. CRISTIAN |
| APPROVED BY | J. J. CRISTIAN |

ETD - POSTING / COMPONENT BOARD DETAILS

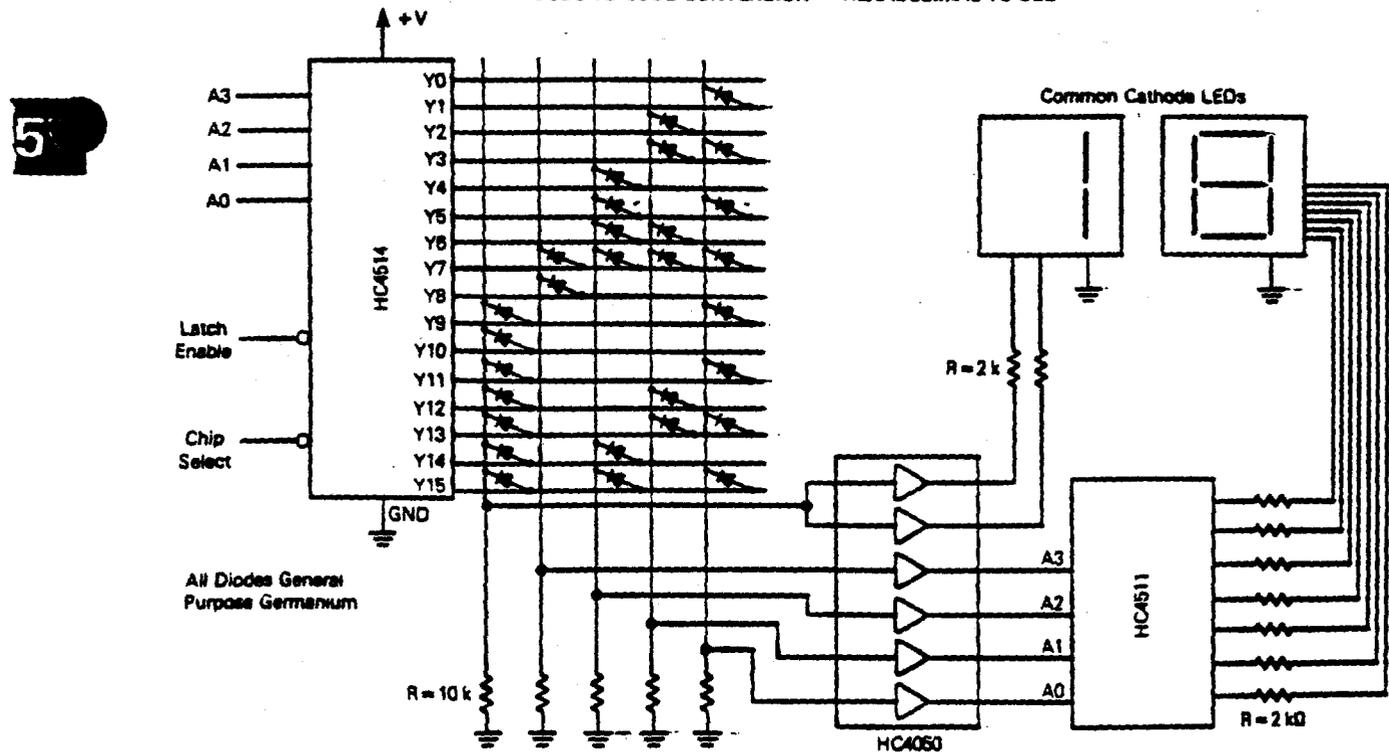
1/1/70

MC54/74HC4514

MICROPROCESSOR MEMORY DECODING



CODE TO CODE CONVERSION - HEXADECIMAL TO BCD



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